

EMI Reduction and PCB Layout Techniques Application Note

Introduction

This application note is intended to recommend methods to reduce electromagnetic interference (EMI) by using careful board layout and routing techniques. In advanced systems, where timing is important, good electrical design practices will minimize EMI, cross talk, and overall performance problems. Noise is harmful because it can result in data corruption and false switching in downstream devices. Good design practices are essential in meeting EMI and ESD requirements, and to achieve maximum line performance. These practices minimize high-speed digital switching noise, common-mode noise, and provide shielding between internal circuits and the environment.

PCB Design Layout Guidelines

We suggest leaving as much copper on the PCB as possible for all power distribution traces. This is critical in all ground traces to avoid ground loops and ground potential problems. It is generally a good practice to fill in unused areas of the signal planes with solid copper and attach them with vias to a ground plane.

Decoupling provides a method to distance circuit functions from the power bus serving that circuit by using decoupling capacitors, ferrite beads and proper printed circuit board layout. Incorrect or insufficient decoupling increases both radiated and conducted emissions that increase both electrical noise and susceptibility to circuit failure.

Use one high-speed, low ESR (0.1 μ F or 0.01 μ F) decoupling capacitor (either an X7R or BX type dielectric ceramic chip) on each power supply pin to ground to reduce high-frequency noise on the power and ground planes. They should be placed next to and on the same side of the PCB as each IC device. Place the de-coupling capacitor, as close to the power pin as possible, to get better noise filtering. Locate the capacitors no more than 10 mils from each IC package's ground pin. Use bulk capacitors (10-22 μ F) between the power and ground planes to minimize switching noise, particularly near high-speed busses.

Provide ample power and ground planes. Route the high-speed signals between parallel ground traces or unbroken ground plane. Keep power and ground noise levels below 50 mV.

Ensure that the power supply is rated for the load and that output ripple is minimal (<50 mV).

At high speeds, signal traces look more like transmission lines where trace impedance becomes an important factor. Paying careful attention to trace lengths and routing will preserve signal rise and fall times and will prevent impedance caused ringing. When routing clock traces, make sure all corners of this trace are rounded. Do not use 90-degree sharp corners or "T" crosses. Terminate the high frequency line with the proper load. If possible, use differential signals, since they will tend to reduce EMI.

Shielding is another effective method to decrease EMI. Avoid breaks in the ground plane, especially in areas where it is shielding high-frequency signals.

Filters (like ferrite beads, bypass capacitors and feedthrough capacitors) are effective ways to reduce power supply noise. Ferrite beads suppress higher frequency noise by adding inductance. Use a single ground plane on PCB design. Keep ferrite bead currents under 65% of the rated load.

The clock should be placed near the center of the board and near a chassis ground. Clock traces should not intersect each other. Do not run long clock traces parallel with other traces, since this will induce crosstalk. All clock signals must be hand-routed before any other signals.

Differential Signal Layout Guidelines

Layout techniques for the differential signals are as follows:

- Route differential pairs close together and away from everything else.
- Keep both traces of each differential pair as close to the same length as possible
- Avoid via and layer changes.
- Avoid crossing each pair with neighboring pairs.
- Eliminate right angles and "T" crosses.
- Keep transmit and receive pairs away from each other. Run orthogonal, or separate with a ground plane.
- Place all the transmit termination components on one side of the board and all the receive components on the other side to maintain transmit and receive separation.

Design Considerations

Device Speed:

- Use lower frequency clocks.
- Use slower rise times.
- Sine waves are preferred over square waves due to a reduction of harmonic energy.

Digital switching noise and power supply ripple are usually created by:

- Overloaded or poorly regulated power supplies.
- De-coupling capacitors far away power pins cause poor de-coupling.
- DC-to-DC converters.

The guidelines suggested in Table 1 are for evaluating acceptable noise levels on the power and ground planes:

Table 1. Criteria for Power Noise Levels (Noise Level Acceptability)

Under 50 mV	Acceptable
50 mV to 100 mV	Marginally Acceptable
Above 100 mV	Unacceptable

Noise Reduction Techniques

Place I/O drivers near where they leave the board.

Place the clock near the epicenter of the devices being driven by that clock. Clock signals that are transmitted off the board should have a buffer placed near the edge of the board closest to the connector pin.

Keep the clock circuit as far away from I/O cables as possible.

Minimize power supply loops by keeping the power supply pins for the clock next to the ground pins.

Keep digital and analog lines separate and route the signals away from each other.

Keep digital and clock signal lines as far away from voltage reference and analog input pins as possible.

Keep the length of sensitive leads, such as decoupling capacitors, as short as possible.

Keep noisy and quiet leads separate.

Keep high-speed lines short and direct.

If the design utilizes Op Amps, terminate any unused Op Amps in dual and quad packs by grounding the positive input and connecting the negative input to the output.

All of the important traces should have a wider trace and need to be guarded with a ground on each side of the trace. Wider traces reduce trace inductance.

Divide the circuits on the board based on their frequency and current switching levels.

Using twisted pair leads will minimize the effects of mutual coupling.

Filter all signals entering the board and filter all signals leaving a noisy environment.

Place a ground lead between low-level signal leads and noisy leads in the same connector like a ribbon cable.

Do not run traces under the crystal or the clock.

Place the crystals flush to the board and ground them.

Do not run sensitive traces parallel with high current, fast switching signals.

Use all power and ground pins of an IC.

Keep power and ground leads parallel and adjacent to each other.