

Introduction

This application note is intended to demonstrate the use of the demo/eval board for the TSLI T231 (or T231-HS) high frequency VCXO IC. TSLI's high performance family of VCXO clock generators is ideally suited for a wide range of applications in which cost, size, power and the number of discrete components need to be minimized. These ICs are designed to exhibit excellent temperature stability and phase noise performance, The T231/T231-HS feature fundamental crystal operation over a frequency range that includes SONET and other communications protocols.

Background

The typical tuning frequency range for the T231/T231-HS is ± 50 ppm. This is, of course, dependent on the design of the crystal, the variable capacitance of the varactor loading the VCXO and the capacitance loading of the printed circuit board (see Application Note AN-104 for a more detailed discussion of tuning frequency range). Page 3 of the T231 data sheet also has a good discussion of tuning range and the impact of various capacitance loading factors. The demo board will also allow measurement, with proper test equipment, of the phase noise characteristics of the VCXO. The T231 is specified to meet -135 dBc/Hz (min) phase noise, at 100 KHz offset from the center frequency. The T231-HS is specified to meet -145 dBc/Hz (min) under the same conditions and is well suited for applications requiring superior phase noise characteristics.

The T231/T231-HS block diagram

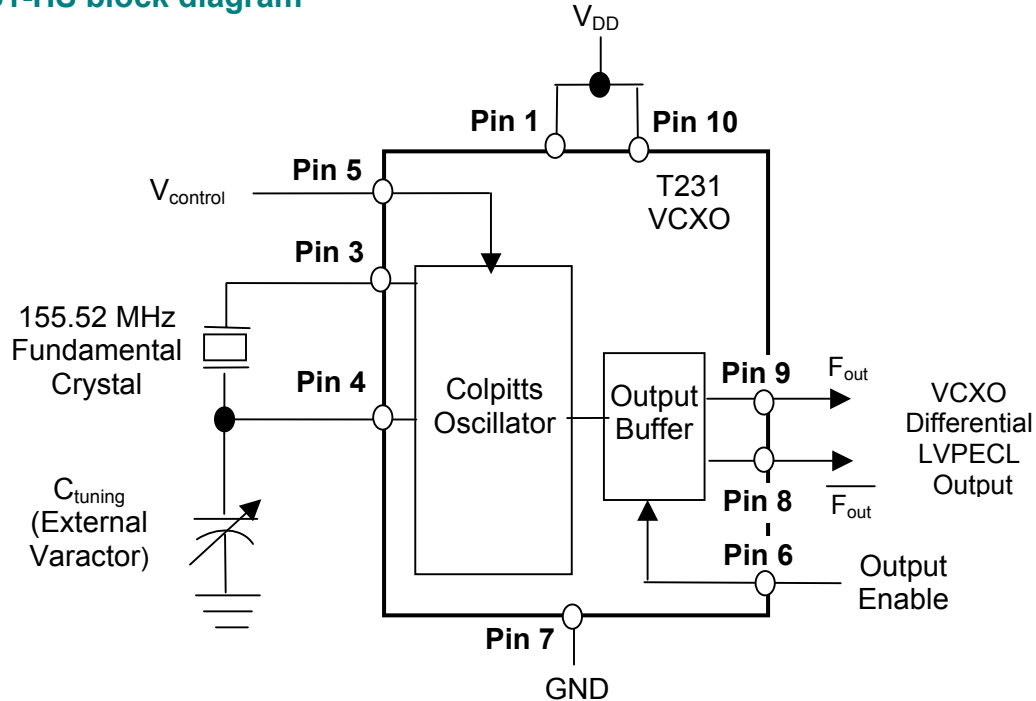


Figure 1. T231/T231-HS VCXO Block Diagram

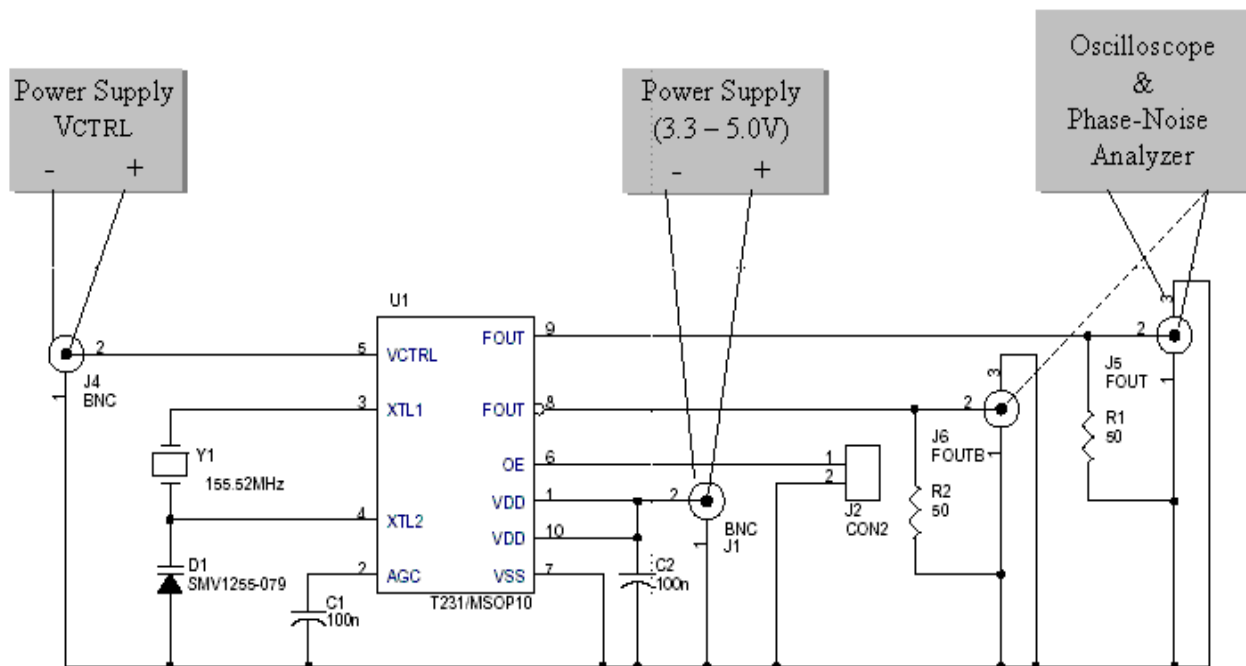


Figure 2. T231/T231-HS VCXO Demo Board Schematic and Test Setup

The T231/T231-HS demo board has a 155.52 MHz fundamental crystal installed for evaluation purposes since this is a popular frequency required for SONET (OC-3) applications. In the above test setup, The V_{control} input (J4) provides the voltage necessary to adjust the capacitance of the varactor diode (D1). Varying the capacitance of the varactor diode from minimum to maximum capacitance results in the adjustment of the output frequency of the VCXO by approximately ± 50 ppm.

Following are plots of the phase noise and the transient output waveform of the T231 using the above test setup. The phase noise was measured using the PN9000 Phase-Noise Measurement System from Aeroflex™, Incorporated. The output transient results were measured using a LeCroy™ SDA6000 Serial Data Analyzer (Oscilloscope). As mentioned above, the nominal VCXO output frequency is 155.52 MHz. The user should take care, when performing these measurements, to keep lead lengths to a minimum to avoid any unnecessary noise pickup. In addition, one should be careful not to inject unwanted noise through the V_{DD} or V_{control} power supplies.

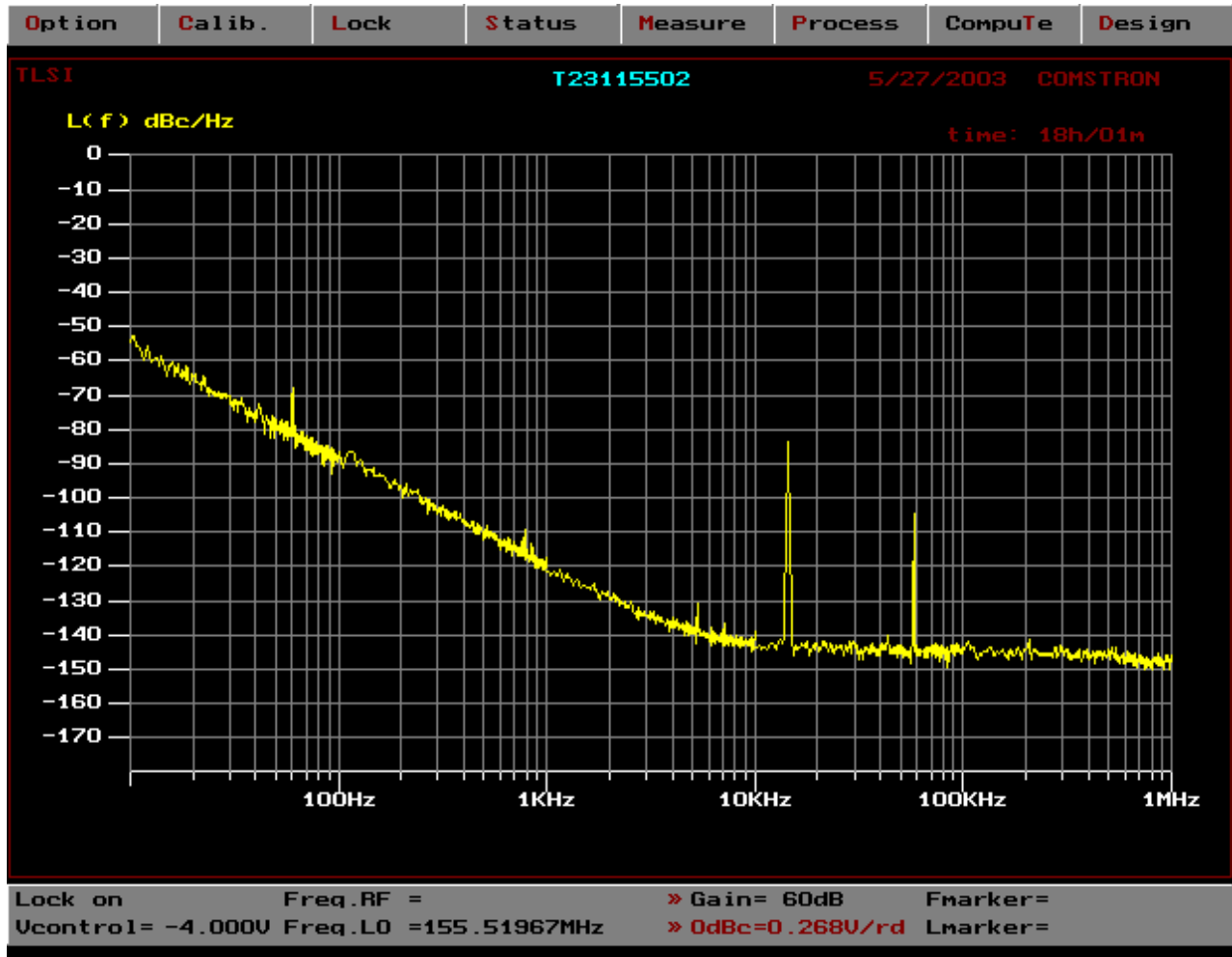


Figure 3. T231-HS VCXO Phase Noise Plot

The above phase noise plot (frequency domain) demonstrates the excellent phase noise performance of the T231-HS, typically -145 dBc/Hz at a 100 kHz offset from the desired frequency (155.52 MHz). The noise artifacts (spikes) shown are not generated by the VCXO but are rather the result of noise pickup by the test setup.

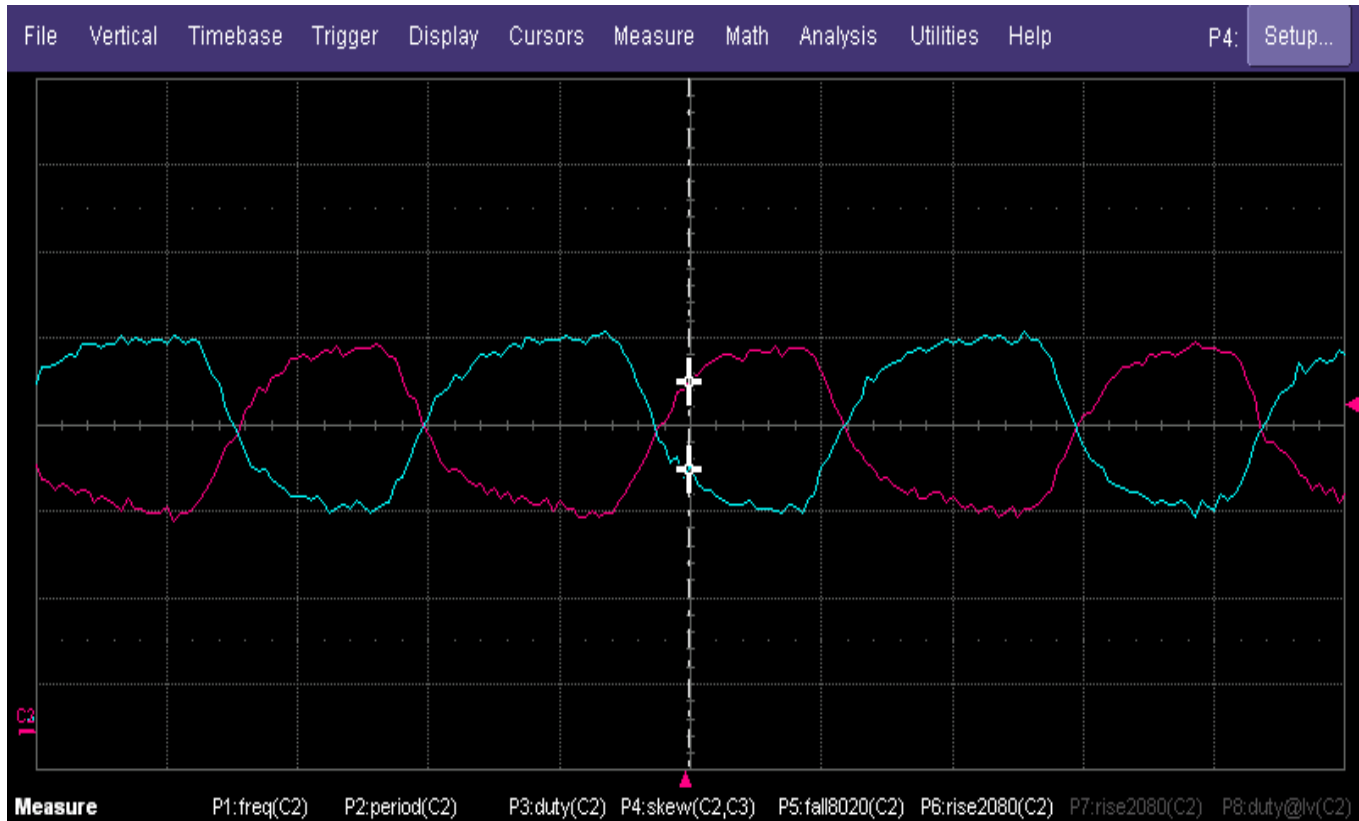


Figure 4. T231-HS VCXO Transient Output Waveform Plot

The above transient output waveform plot demonstrates the output frequency running at 155.52 MHz with a PECL output swing (800 mV). **Note:** In the demo board setup, the two complementary outputs are directly terminated with 50 Ohms to ground, respectively, which is not a true PECL termination. They should be referenced to VDD/2 rather than to ground. For this reason, as can be seen above, the duty-cycle is about 44%. This is not an anomaly of the T231-HS VCXO but is rather an error in the design of the demo board. This will be corrected in the near future. Accordingly, this duty cycle issue will not be present when the T231 outputs are properly terminated using a true PECL setup with the outputs referenced to VDD/2. The output rise-time and fall-time are 810ps and 730ps, respectively.

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