

T277

VCXO Clock Generator IC

8 MHz to 100 MHz

P R E L I M I N A R Y

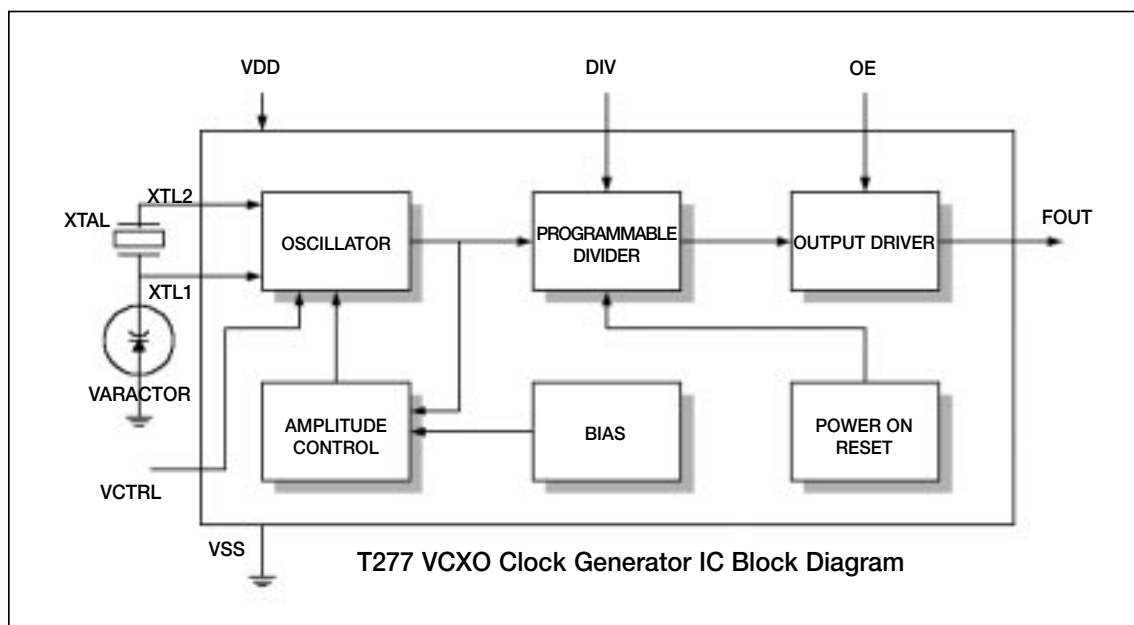
GENERAL DESCRIPTION

TLSI's family of VCXO Clock Generators is ideally suited for a wide range of applications in which cost, size, power, and the number of discrete components need to be minimized. These ICs are designed to exhibit excellent temperature stability and phase noise performance. The device incorporates a programmable divider that allows the user to select output frequencies lower than the crystal frequency while providing 50% output symmetry. Typical tuning frequency range is ± 200 PPM (crystal and varactor dependent). The devices are available as die, probed wafers, or in surface-mount packages.

FEATURES

- Crystal Frequency Range 8 MHz to 100 MHz
- Supply Voltage 3 V to 5.5 V
- Operating Temperature -40°C to $+85^{\circ}\text{C}$
- Power less than 150 mW
- Start-Up Time less than 5 mS
- Phase Noise at 100 KHz Offset from F_c less than -140 dBc/Hz
- Rise and Fall Times less than 3 nS
- Programmable Frequency Division: 1, 4, 16
- Nominal Output Duty Cycle 45% to 55%
- Output Drive Capability of 50 pF
- Tuning Input Impedance $50\text{ K}\Omega$
- Internal Crystal Load Capacitance 20 pF

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

* Operation of the device at or beyond these specifications may result in permanent damage or affect operation and reliability of the product.

PARAMETER	CONDITIONS	UNITS
Supply Voltage	$V_{SS} - 0.5 \leq V_{DD} \leq 6.0$	V
DC Input Voltage	$V_{SS} - 0.5 \leq V_{IN} \leq V_{DD} + 0.5$	V
DC Output Voltage	$V_{SS} - 0.5 \leq V_{OUT} \leq V_{DD} + 0.5$	V
Storage Temperature	$-65 < T_S < +150$	°C
Ambient Temperature	$-40 < T_A < +85$	°C
Junction Temperature	$-65 < T_J < +125$	°C
Soldering Temperature	$T_{SLDR} < 260$ for less than 10 seconds	°C

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

$V_{DD} = 5.0$ V, -40 °C $< T_A < +85$ °C unless otherwise specified

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage		V_{DD}	3.0	5.0	5.5	V
High-Level Output Voltage	$I_{OH} = -1$ mA	V_{OH}	4.5			V
Low-Level Output Voltage	$I_{OL} = 20$ mA	V_{OL}			0.5	V
High-Level Input Voltage		V_{IH}	1.0			
Low-Level Input Voltage		V_{IL}			4.0	V
OE High-Level Input Current		I_{IH}			1.0	μA
OE Low-Level Input Current		I_{OL}		-50		μA
DIV High-Level Input Current	DIV = V_{DD}	I_{IH}		50		μA
DIV Low-Level Input Current	DIV = V_{SS}	I_{OL}		-50		μA
Supply Current	F=20 MHz, $C_L=50$ pf, DIV = OPEN	I_{DD}		8.5	13.0	mA
Tuning Range (See Tuning Range Section)		Δf		±200		ppm
Crystal Drive		V_{XTL}		1.0		V pp
High-Level Output Source Current	$V_{OH} = 4.0$ V	I_{OH}		-60		mA
Low-Level Output Sink Current	$V_{OL} = 1.0$ V	I_{OL}		60		mA
Short-Circuit Source Current	< 60 seconds	I_{OSH}			-40	mA
Short-Circuit Sink Current	< 60 seconds	I_{OSL}	40			mA

AC CHARACTERISTICS

$V_{DD} = 5.0$ V, -40 °C $< T_A < +85$ °C unless otherwise specified

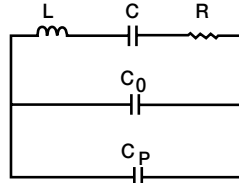
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Crystal Frequency Range		F_{XTL}	8.0		100.0	MHz
Output Duty Cycle		ODC	45		55	%
Power-Up Interval		T_{ON}		2.5	5.0	ms
Output Jitter	RMS, 12kHz to 10MHz	J_O			1	ps
Rise and Fall Time	$C_L=25$ pF	t_r, t_f		3		ns
Phase Noise	100 kHz offset from F_c	N_{PH}			-140	dBc/Hz
Temperature Stability		ΔF_{TEMP}		±15		ppm
Frequency vs. Load Capacitance		ΔF_{LC}		1		ppm
Frequency vs. Supply Voltage	$V_{DD} \pm 15\%$	ΔF_{SV}		1		ppm
Tuning Input Impedance		Z_{TUNE}		50	100	KΩ

TUNING RANGE

Tuning Range depends on the design of the crystal and the capacitance loading of the printed circuit board and the variable capacitance loading the T277 IC. The parallel resonant frequency of the crystal with any external capacitive loading is greater than the fixed series resonant frequency of the crystal by Δf :

$$\Delta f = C \times 10^6 / 2(C_0 + C_p) \text{ ppm}$$

where C is the series mechanical capacitance of the crystal, C_0 is the parallel capacitance of the filter, and C_p is the additional loading capacitance used to tune the crystal. The loading capacitance is the equivalent capacitance of the 20 pF chip internal load capacitance in series with the varactor capacitance. All capacitances are in units of picofarads.



Oscillator Equivalent Circuit

Example: For a typical crystal, $C = 0.02$ pf and $C_0 = 5$ pf. Using a Hyperabrupt Tuning Diode, the typical capacitance of the diode is 12.3 pF at 1 volt and 2.60 pF at 3 volts. The varactor diode appears in series with the 20 pF internal chip capacitance. In addition, assuming 2 pF stray board wiring capacitance across both the varactor and the chip terminals, the following calculations determine the pullability of the oscillator:

Frequency shift with 1 volt across the varactor diode:

$$C_p = 20 \text{ pF} + 2 \text{ pF in series with } 12.3 \text{ pF} + 2 \text{ pF} = (22.0 \times 14.3) / (22.0 + 14.3) \text{ pF} = 8.67 \text{ pF}$$

$$\Delta f_1 = 0.02 \times 10^6 / (2(5 + 8.67)) \text{ ppm} = 731.5 \text{ ppm}$$

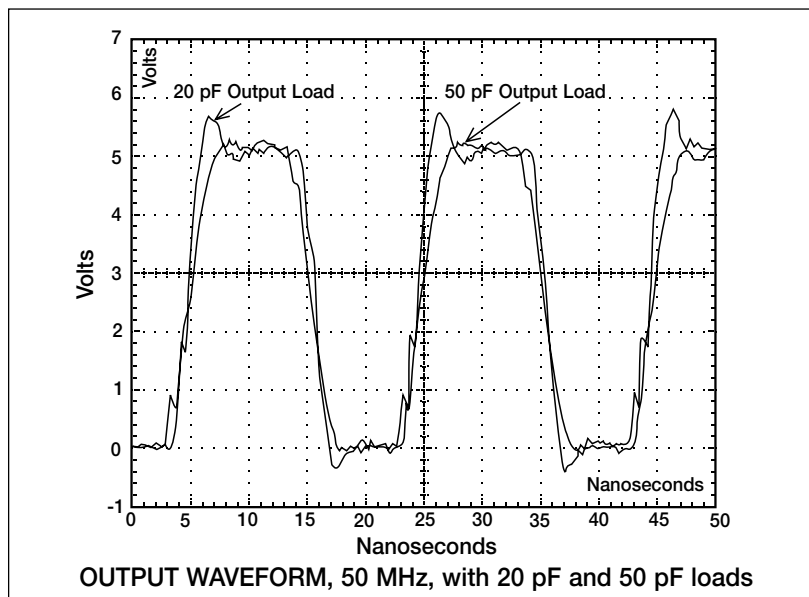
Frequency shift with 3 volts across the varactor diode:

$$C_p = 20 \text{ pF} + 2 \text{ pF in series with } 2.60 \text{ pF} + 2 \text{ pF} = (22.0 \times 4.60) / (22.0 + 4.60) \text{ pF} = 3.80 \text{ pF}$$

$$\Delta f_2 = 0.02 \times 10^6 / (2(5 + 3.80)) \text{ ppm} = 1136.4 \text{ ppm}$$

$$\text{Total Tuning Range} = \Delta f_2 - \Delta f_1 = 1136.4 \text{ ppm} - 731.5 \text{ ppm} = 405 \text{ ppm}$$

OUTPUT WAVEFORMS

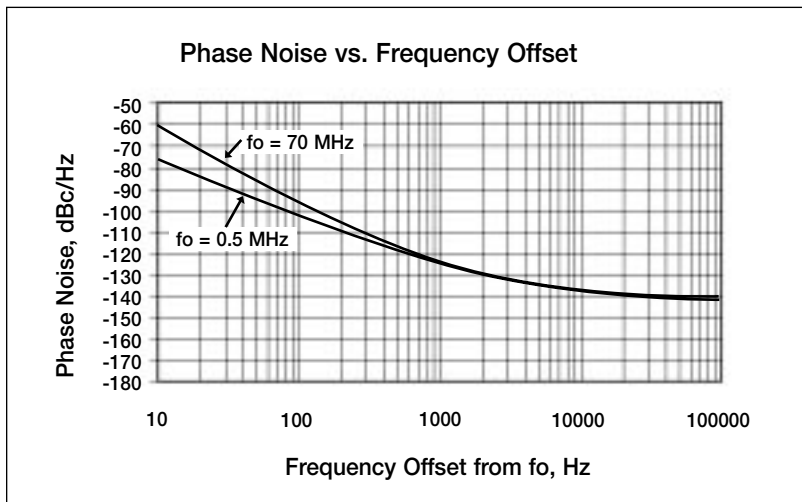
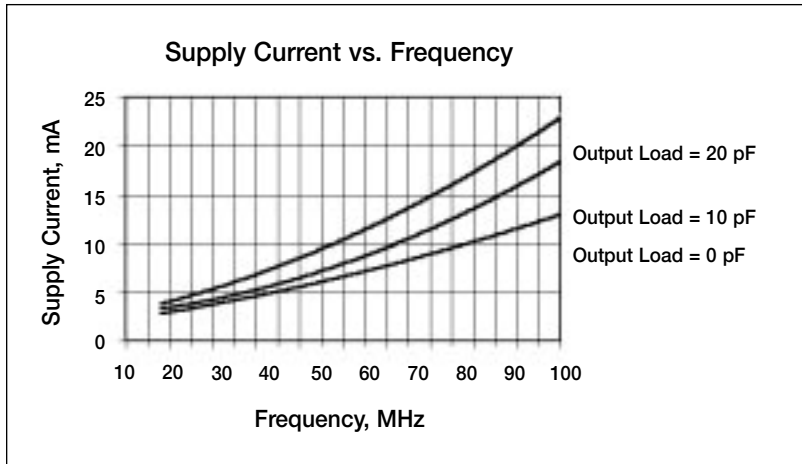
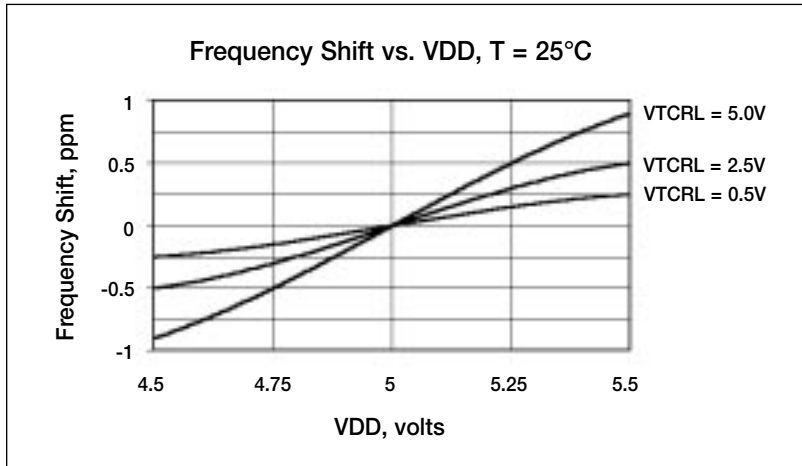


DIVIDER MODES

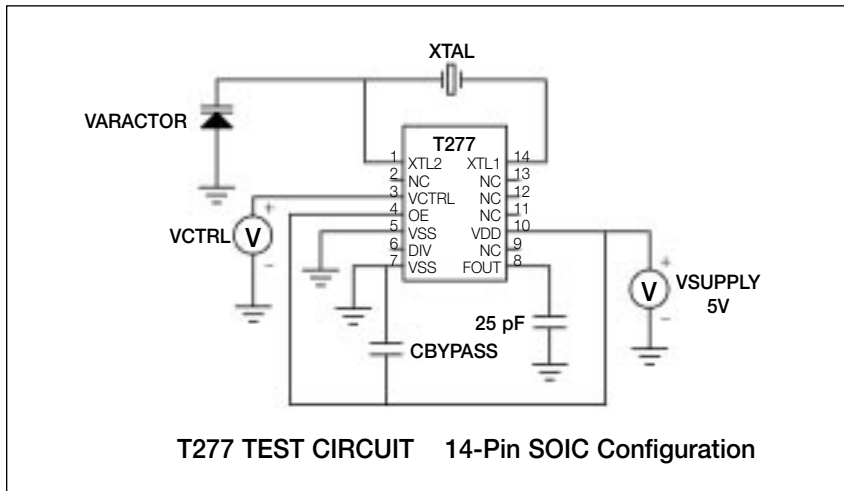
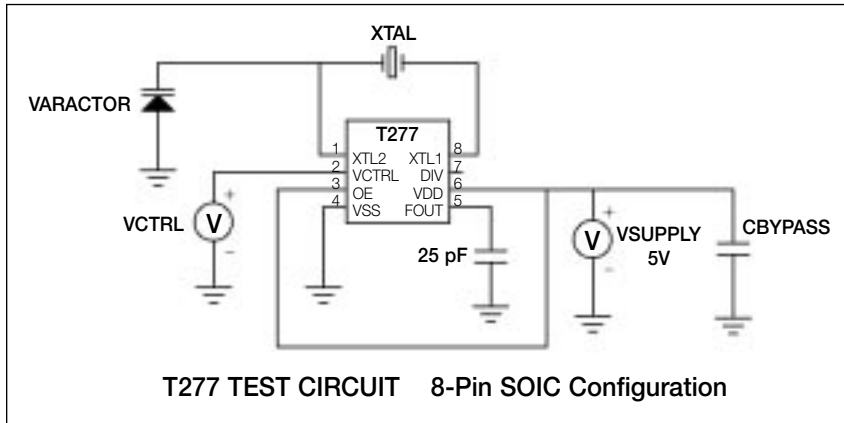
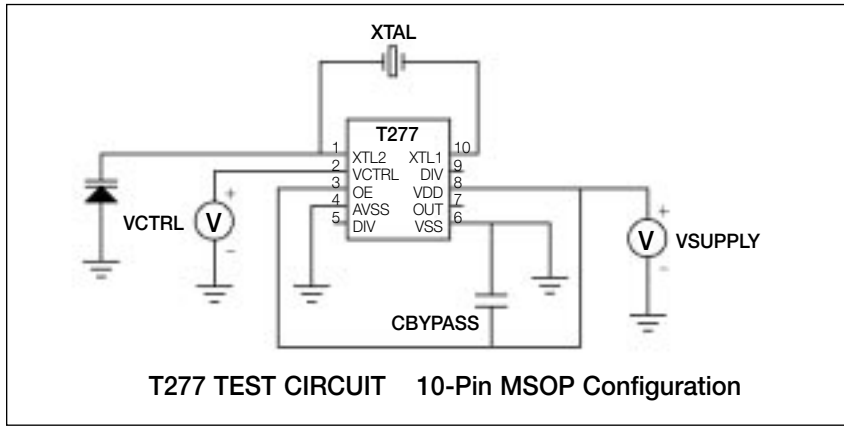
Undivided Crystal Frequency = F_{XTL}

DIV	FOUT
OPEN	F_{XTL}
V_{SS}	$F_{XTL}/4$
V_{DD}	$F_{XTL}/16$

GRAPHS OF TYPICAL OPERATING CONDITIONS

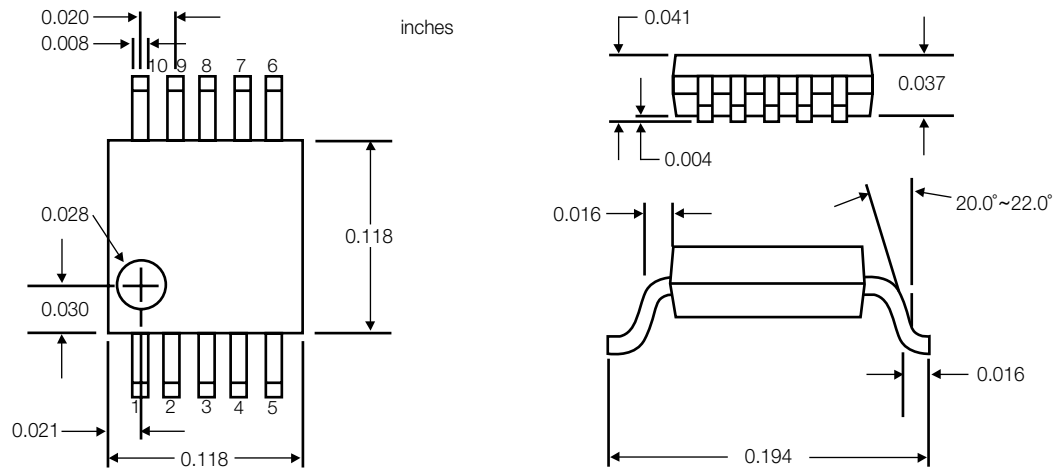


TEST CIRCUIT SCHEMATIC

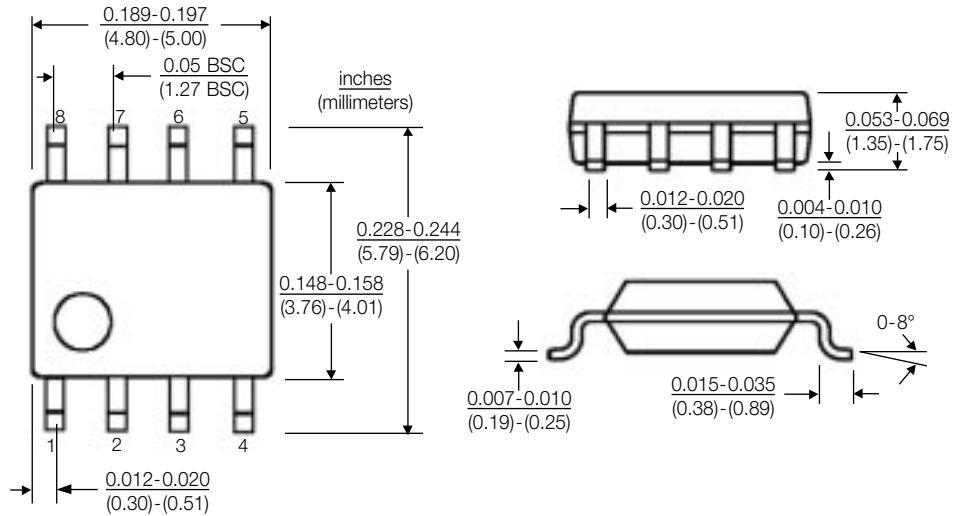


PACKAGE INFORMATION

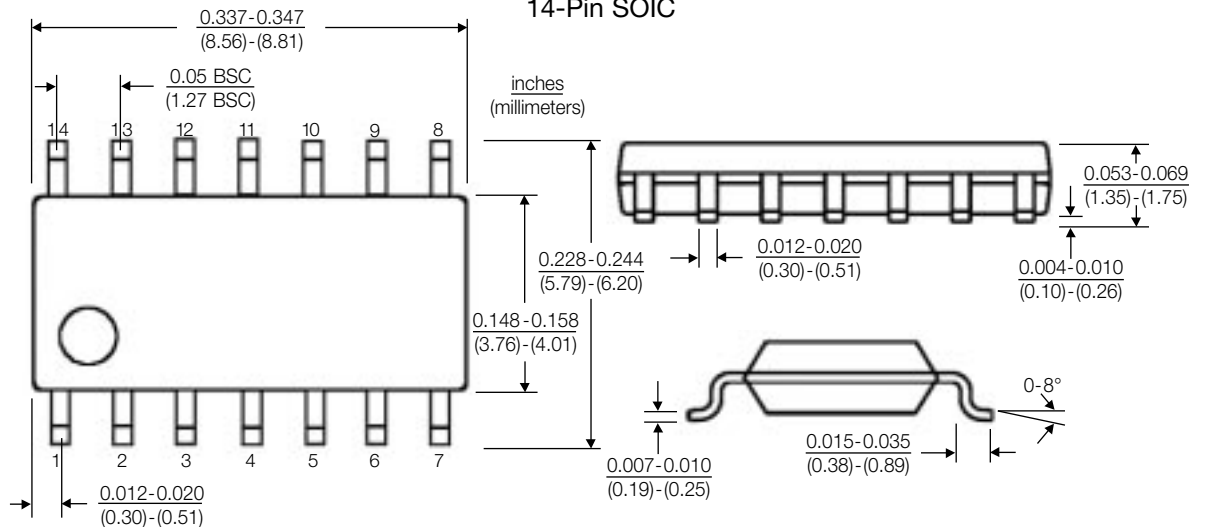
10-Pin MSOP



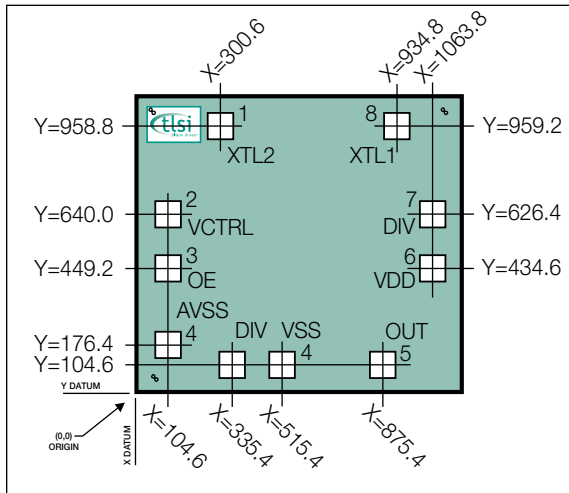
8-Pin SOIC



14-Pin SOIC



DIE SIZE



NOTES:

- 1) All dimensions are in microns.
- 2) Standard pad size = 92 X 92 microns.
- 3) The (0,0) origin is located on the outside edge of the inner scribe.
- 4) Substrate = VSS

PIN FUNCTIONS

10-Pin MSOP

NUMBER	NAME	FUNCTION
1	XTL2	Crystal Connection, Lead 2
2	VCTRL	Frequency Control, 0.5 to 3 Volts
3	OE	Output Enable
4	AVSS	Power Supply Reference
5	DIV	Divider Program Pin
6	VSS	Power Supply Reference
7	OUT	Output
8	VDD	Power Supply
9	DIV	Internally Connected to Pin 5
10	XTL1	Crystal Connection, Lead 1

8-Pin SOIC

NUMBER	NAME	FUNCTION
1	XTL2	Crystal Connection, Lead 2
2	VCTRL	Frequency Control, 0.5 to 3 Volts
3	OE	Output Enable
4	VSS	Power Supply Reference
5	FOUT	Output
6	VDD	Power Supply
7	DIV	Divider Programming Pin
8	XTL1	Crystal Connection, Lead 1

PIN FUNCTIONS CONTINUED

14-Pin SOIC

NUMBER	NAME	FUNCTION
1	XTL2	Crystal Connection, Lead 2
2	NC	No Connection
3	VCTRL	Frequency Control, 0.5 to 3 Volts
4	OE	Output Enable
5	VSS	Power Supply Reference
6	DIV	Divider Programming Pin
7	VSS	Power Supply Reference
8	FOUT	Output
9	NC	No Connection
10	VDD	Power Supply
11	NC	No Connection
12	NC	No Connection
13	NC	No Connection
14	XTL1	Crystal Connection, Lead 1

ORDERING INFORMATION

PART NUMBER	PACKAGE
T277-DPW	Die-Probed Wafer
T277-DIE	Die-Waffle Pack
T277-M10	10-Pin MSOP
T277-S08	8-Pin SOIC
T277-S14	14-Pin SOIC

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