



# T73LVP23

## Dual 3.3V Differential LVPECL-to-LVTTL/LVCMOS Translator

### Applications

- Multiple LVPECL-to-LVTTL/LVCMOS clock sources

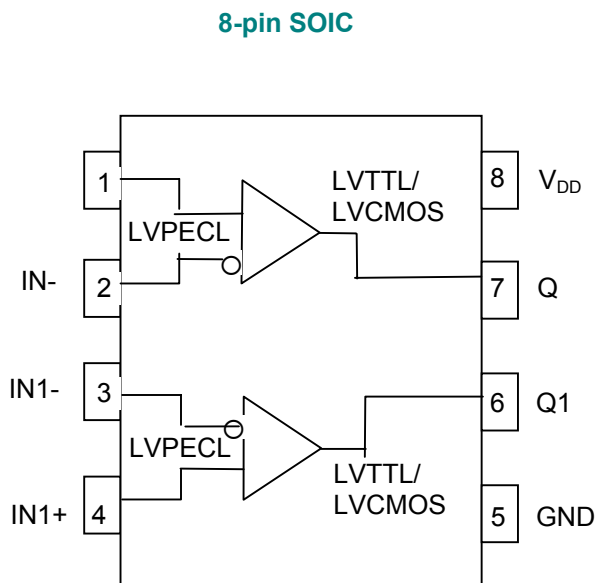
### General Description

The TLSI T73LVP23 is a general purpose dual differential LVPECL-to-LVTTL/LVCMOS translator operating from a single +3.3V supply. The 8-pin SOIC package makes it ideal for applications which require the translation of multiple clocks or data signals, and where cost, performance and size are of critical importance. The T73LVP23 is 100K PECL compatible and is a **Pin-for-pin replacement for the MC100EPT23D**.

### Features

- 1.1 ns Typical Propagation Delay
- Maximum Operating Frequency > 500 MHz
- Operating Temperature -40°C to +85°C
- 24 mA LVTTL/LVCMOS outputs
- Operating Range: VCC = +3.0V to +3.6V
- Open Input Default State
- ESD rating > 2000V (Human Body Model)
- Available in standard 8-pin SOIC package

Figure 1. Functional Block Diagrams & Pin Assignments (Top View)



See page 4 for package outline drawing and ordering information.

Table 1. Pin Descriptions

Name	Description	Type	Pin #
IN <sup>+</sup> ( <sup>1</sup> ), IN <sup>-</sup> ( <sup>1</sup> )	LVPECL differential input pair	I	1, 2
IN1 <sup>-</sup> ( <sup>1</sup> ), IN1 <sup>+</sup> ( <sup>1</sup> )	LVPECL differential input pair	I	3, 4
GND	Connect to ground	P	5
Q, Q1	LVTTL/LVCMOS outputs	O	7, 6
V <sub>DD</sub>	Positive supply – connect to +3.3V	P	8

**Type Legend:** I = Input  
O = Output  
P = Power supply connection

**Notes:** 1. Q, Q1 outputs default LOW when IN<sup>+</sup>, IN<sup>-</sup> and IN1<sup>+</sup>, IN1<sup>-</sup> are left open.

Table 2. Absolute Maximum Ratings (each channel)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V <sub>DD</sub>	Supply voltage	Referenced to GND			+5.0	V
V <sub>IN</sub>	Input voltage	Referenced to GND	-0.5		V <sub>DD</sub>	V
I <sub>OUT</sub>	Output current in LOW state	Continuous			50	mA
T <sub>STG</sub>	Storage temperature		-65		+150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3. Operating Conditions (each channel)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V <sub>DD</sub>	Power Supply Voltage		+3.0	+3.3	+3.6	V
T <sub>A</sub>	Ambient Temperature		-40		+85	°C
V <sub>IH</sub>	Input HIGH Voltage	Single-ended	+2.10		+2.42	V
V <sub>IL</sub>	Input LOW Voltage	Single-ended	+1.35		+1.68	V

**Table 4. DC Characteristics (each channel)**

$T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = +3.0\text{V}$  to  $+3.6\text{V}$  unless otherwise stated below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{IH}$	Input HIGH Current	Single-ended			60	$\mu\text{A}$
$I_{IL}$	Input LOW Current	Single-ended			0.5	$\mu\text{A}$
$V_{CMR}$	Common mode input range	Differential	2.0		$V_{DD}$	V
$V_{OH}$	Output HIGH Voltage <sup>(1)</sup>	$I_{OH} = -3.0\text{ mA}$	2.4			V
$V_{OL}$	Output LOW Voltage <sup>(1)</sup>	$I_{OL} = 24\text{ mA}$			0.5	V
$I_{DD}$	Power Supply Current	Output set to HIGH, no load, both channels total		18	24	mA
$I_{OS}$	Output short circuit current		-200		-80	mA

**Notes:** 1. The T73LVP23 is designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board.

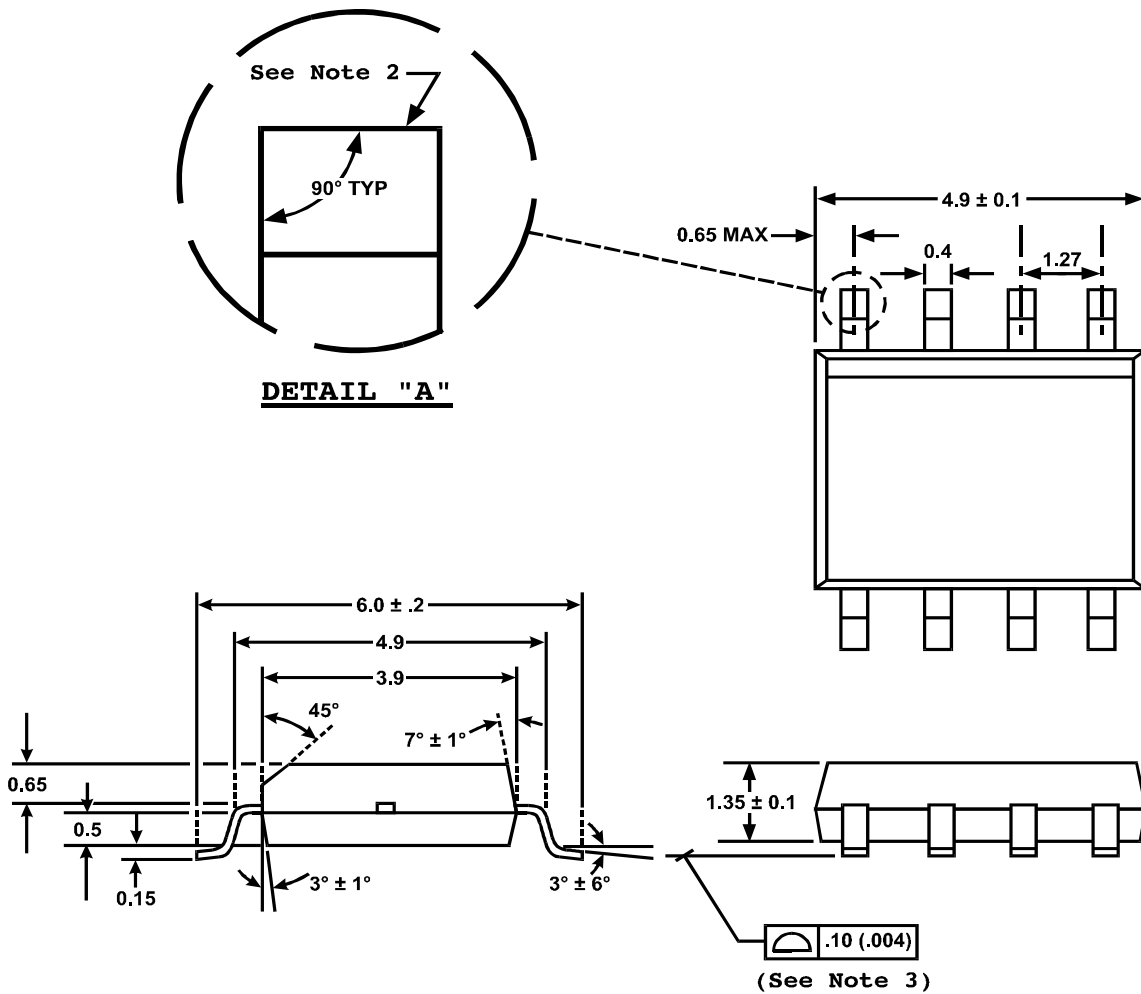
**Table 5. AC Characteristics<sup>(1)</sup> (each channel)**

$T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = +3.0\text{V}$  to  $+3.6\text{V}$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{PP}$	Peak-to-peak input		150			mV
$t_{PLH}$	Propagation Delay	$C_L = 20\text{ pF}$		1.0	1.2	ns
$t_{PHL}$	Propagation Delay	$C_L = 20\text{ pF}$		1.0	1.2	ns
$t_r/t_f$	Output Rise/Fall time	0.8V – 2.0V		500		ps
$f_{MAX}$	Maximum Input Frequency			500		MHz

**Notes:** 1. Measured using a 750mV peak-to-peak, 50% duty cycle clock source.  $R_L = 500\Omega$  to GND and  $C_L = 20\text{ pF}$  to GND.

Figure 2. Package Outline (8-pin SOIC)



- Note: 1) All dimensions are in mm.  
 2) All leads must be blunt cut. (See DETAIL "A")  
 3) Lead coplanarity not to exceed 0.004" maximum.

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Table 6. Ordering Information

Part Number	Marking	Shipping/Packaging	No. of Pins	Package	Temperature
T737LVP23-SO8	T73LVP23	Tubes	8	SOIC	-40°C to +85°C
T73LVP23-SO8-TNR	T73LVP23	Tape & Reel	8	SOIC	-40°C to +85°C