

### 1.0 Features

- Phase-Locked Loop (PLL) device synthesizes output clock frequency from crystal or external reference clock
- One-chip tunable voltage controlled crystal oscillator (VCXO) allows precise system frequency tuning
- 3.3V operation
- 8 pin (150 mil) SOIC package
- Uses inexpensive 14pF pullable crystals with no external capacitors required.
- 12mA drive capability at TTL levels
- Very low phase noise PLL

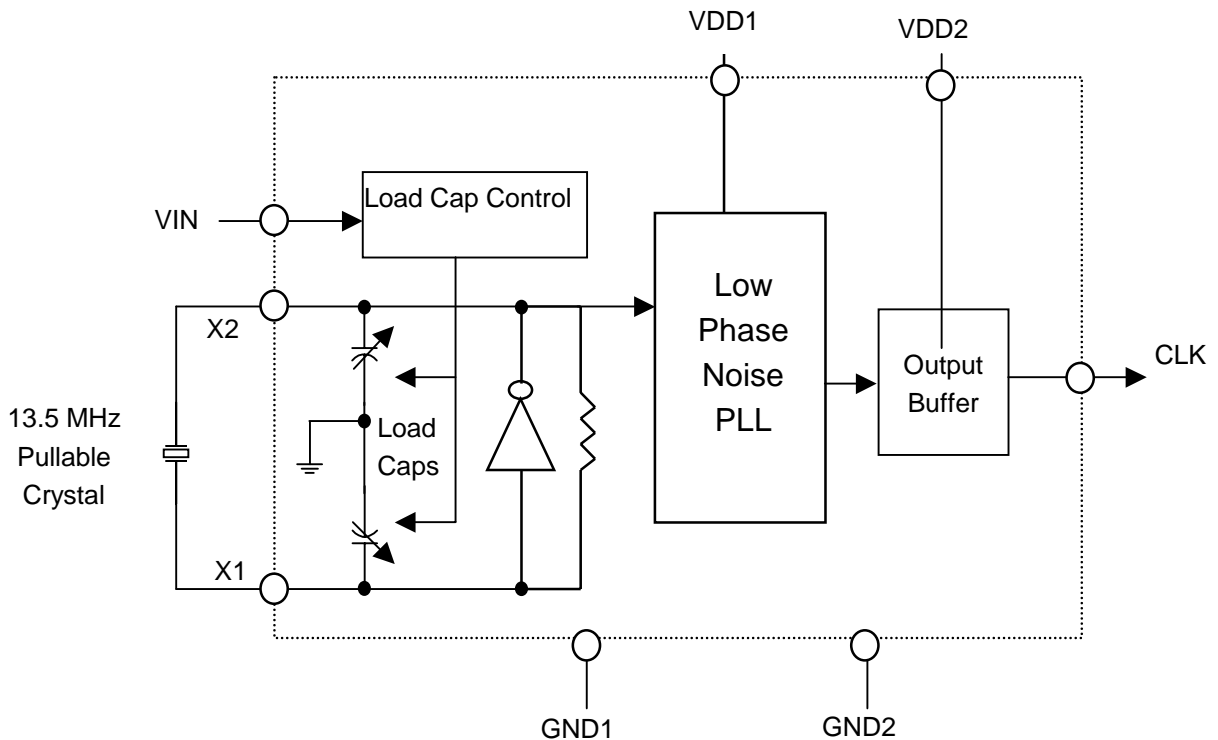
### 2.0 Applications

- Set-top boxes
- MPEG Video clock source
- Oscillator replacement

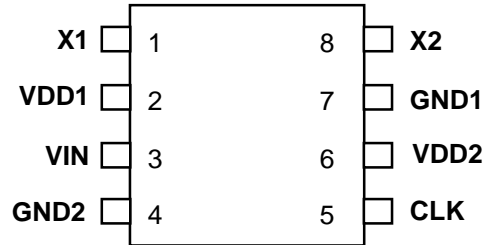
### 3.0 Description

The T83027 is a single-chip, low-jitter Voltage-Controlled-Crystal-Oscillator combined with a low noise Phase Locked Loop. The device accepts a 13.5 MHz, 14 pF crystal, and produces a low jitter 27 MHz output frequency. A 0 to 3.0V control signal is used to fine tune the output clock frequency in the  $\pm 100$ ppm range. This finds use in systems that have frequency matching requirements, such as digital satellite receivers.

Figure 1: Block Diagram



**8-pin (150 mil) SOIC**



**Table 1: Pin Descriptions**

PIN	TYPE	NAME	DESCRIPTION
1	Xi	X1	Crystal Connection. Connect to a 13.5 MHz Pullable Crystal or reference frequency input.
2	P	VDD1	Core $V_{DD}$ . Connect to 3.3V
3	I	VIN	Voltage input to VCXO. Zero to 3V Signal Controls the Frequency of the VCXO.
4	P	GND2	Connect to Ground.
5	O	CLK	Clock Output
6	P	VDD2	Pad Driver $V_{DD}$ . Connect to 3.3V
7	P	GND1	Connect to Ground.
8	Xi	X2	Crystal Connection. Connect to a 13.5 MHz pullable crystal.

Legend: I = Input  
 O = Output  
 P = Power supply connection  
 Xi = Crystal connections.

### 4.0 Functional Block Description

#### 4.1 Voltage Controlled Crystal Oscillator

The VCXO provides a tunable, low-jitter frequency reference. Loading capacitance for the crystal is internal to the T83027. No external components (other than the crystal resonator itself) are required for operation of the VCXO.

Tuning of the VCXO frequency is accomplished by varying the voltage on Vin (Pin 3).

The oscillator operates the crystal resonator in the parallel-resonant mode. Crystal warping, or the “pulling” of the crystal oscillation frequency, is accomplished by altering the effective load capacitance presented to the crystal by the oscillator circuit. The actual amount that changing the load capacitance alters the oscillator frequency will be dependent on the characteristics of the crystal as well as the oscillator circuit itself.

Specifically, the motional capacitance of the crystal (usually referred to by crystal manufacturers as  $C_1$ ), the static capacitance of the crystal ( $C_0$ ), and the load capacitance ( $C_L$ ) of the oscillator determine the “warping” or “pulling” capability of the crystal in the oscillator circuit. A simple formula to obtain the warping capability of a crystal oscillator is:

$$\Delta f (ppm) = \frac{C_1 \times (C_{L2} - C_{L1}) \times 10^6}{2 \times (C_0 + C_{L2}) \times (C_0 + C_{L1})}$$

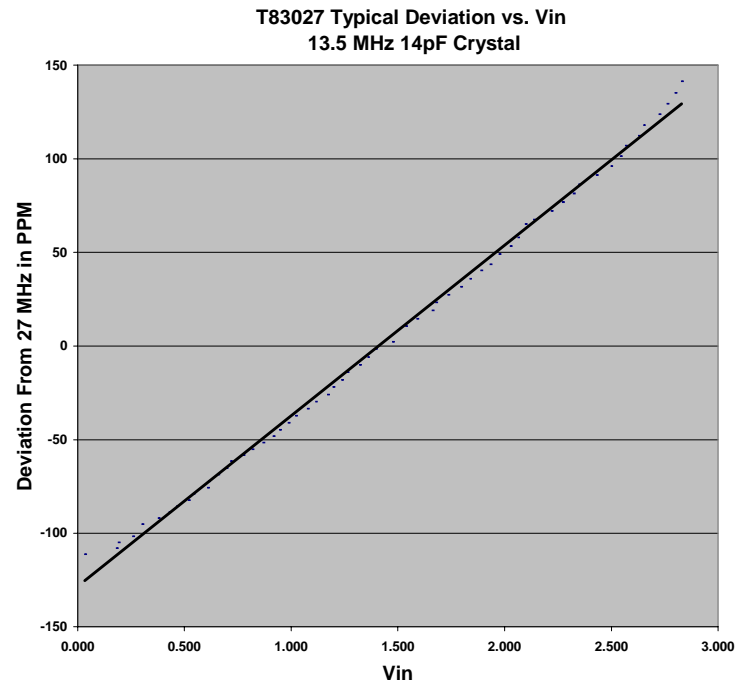
where  $C_{L1}$  and  $C_{L2}$  are the two extremes of the applied load capacitance.

EXAMPLE: A crystal with the following parameters is used. With  $C_1 = 0.025\text{pF}$ ,  $C_0 = 6\text{pF}$ ,  $C_{L1} = 10\text{pF}$ , and  $C_{L2} = 20\text{pF}$ , the tuning range is

$$\Delta f = \frac{0.025 \times (20 - 10) \times 10^6}{2 \times (6 + 20) \times (6 + 10)} = 300 \text{ ppm}.$$

#### 4.2 Phase Locked Loop (PLL)

The on-chip PLL is a standard phase locked loop architecture that multiplies the reference frequency by two. The frequency multiplication is exact with zero synthesis error.



## 5.0 Electrical Specifications

**Table 2: Absolute Maximum Ratings**

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage ( $V_{SS} = \text{ground}$ )	$V_{DD}$	$V_{SS}-0.5$	5	V
Input Voltage, dc	$V_I$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	$V_{SS}-0.5$	$V_{DD}+0.5$	V
Input Clamp Current, dc ( $V_I < 0$ or $V_I > V_{DD}$ )	$I_{IK}$	-25	25	mA
Output Clamp Current, dc ( $V_I < 0$ or $V_I > V_{DD}$ )	$I_{OK}$	-50	50	mA
Storage Temperature Range (non-condensing)	$T_S$	-65	150	°C
Ambient Temperature Range, Under Bias	$T_A$	-55	125	°C
Junction Temperature	$T_J$		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection			2	KV

**Table 3: Operating Conditions**

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Core Supply Voltage ( $V_{DD}$ )	$V_{DD}$		3.15	3.3	3.45	V
VCXO Control Voltage, $V_{IN}$	$V_{IN}$		0		3.0	V
Ambient Operating Temperature Range	$T_A$		0		70	°C
Crystal Resonator Frequency	$f_{XTAL}$	Fundamental Mode	12	13.5	20	MHz

**Table 4: DC Electrical Specifications**

Unless otherwise stated,  $V_{DD} = 3.15V$  to  $3.45V$ , no load on any output, and ambient temperature range  $T_A = 0^{\circ}C$  to  $70^{\circ}C$ .

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic, with no load	$I_{DD}$	$f_{XTAL} = 13.5MHz$ No Load		28		mA
Output High Voltage	$V_{OH}$	$I_{OH} = -12mA$	2.4			V
Output Low Voltage	$V_{OL}$	$I_{OL} = 12mA$			0.4	V
Input Low Current	$I_{IL}$	0 Volts X1 (Pin 1) and VIN (Pin 3) Inputs			-60	$\mu A$
Input High Current	$I_{IH}$	3 Volts X1 (Pin 1) and VIN (Pin 3) Inputs			60	$\mu A$
Short Circuit Current	$I_{OS}$	Clock Output (Pin 5)		$\pm 85$		mA
Input Low Voltage	$V_{IL}$	X1 (Pin 1) being Driven			0.4	V
Input High Voltage	$V_{IH}$	X1 (Pin 1) being Driven	2.5			
<b>Voltage Controlled Crystal Oscillator - VDD=3.3V</b>						
Crystal Loading Capacitance	$C_{L(xtal)}$	As seen by a crystal connected to XIN and XOUT (@ $V_{XTUNE} = 1.65V$ )		14		pF
Crystal Gamma	$C_0/C_1$				240	
VCXO Tuning Range		$f_{XTAL} = 13.5 MHz$ ; $C_{L(xtal)} = 14pF$ gamma = 240; (peak-to peak)	200	250		ppm
VCXO Tuning Characteristic		Note: positive $\Delta F$ for positive $\Delta V$		75		ppm/V
Crystal ESR					35	$\Omega$

**Table 5: AC Timing Specifications**

Unless otherwise stated,  $V_{DD} = 3.15V$  to  $3.45V$ , no load on any output, and ambient temperature range  $T_A = 0^{\circ}C$  to  $70^{\circ}C$ . Parameters denoted with an asterisk ( \* ) represent nominal characterization data and are not production tested to any specific limits.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
<b>Clock Output (CLK)</b>						
Duty Cycle *		Ratio of high pulse width (as measured from rising edge to next falling edge at $V_{DD}/2$ ) to one clock period	40		60	%
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to next rising edge at $V_{DD}/2$ , $C_L = 10pF$ ; $f_{XTAL} = 13.5 MHz$		$\pm 70$		ps
Phase Noise		$f_{XTAL} = 13.5 MHz$ : Offset Frequency = 100KHz		-100		dBc
Rise Time *	$t_r$	Measured 0.8V to 2.0V, $C_L = 10pF$			1.5	ns
Fall Time *	$t_f$	Measured 2.0V to 0.8V; $C_L = 10pF$			1.5	ns



# T83027

## PLL Clock Generator IC with VCXO

### 6.0 Ordering Information

ORDERING PART NUMBER	PACKAGE TYPE	SHIPPING CONFIGURATION
<b>T83027-S08</b>	8-pin SOIC	Tubes
<b>T83027-S08-TNR</b>	8-pin SOIC	Tape and Reel
<b>T83027-DIE</b>	DIE	Waffle-Pack

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