



## Low Skew, 1-to-16 Differential to 2.5V LVPECL Fanout Buffer

### Applications

- Clock distribution applications in telecommunications, networking and computing systems

### General Description

The T8530 is a low skew, high performance 1-to-16 Differential to 2.5V LVPECL fanout buffer. The differential input can accept most standard differential input levels. The T8530 produces sixteen 2.5V LVPECL differential output pairs. The high gain differential input amplifier accepts peak-to-peak levels as small as 150mV, as long as the common mode voltage is within specification. T8530 is ideal for those clock distribution applications demanding high performance and repeatability.

### Features

- 16 differential 2.5V LVPECL outputs
- CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Maximum operating frequency: 500MHz
- Translates any single-ended input signal to 2.5V LVPECL levels with a resistor bias on nCLK input
- Output skew: 50ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 2ns (maximum)
- 3.3V core, 2.5V output operating supply
- 0°C to +70°C ambient operating temperature range
- Pin-for-pin compatible with ICS8530

Figure 1. Functional Block Diagram

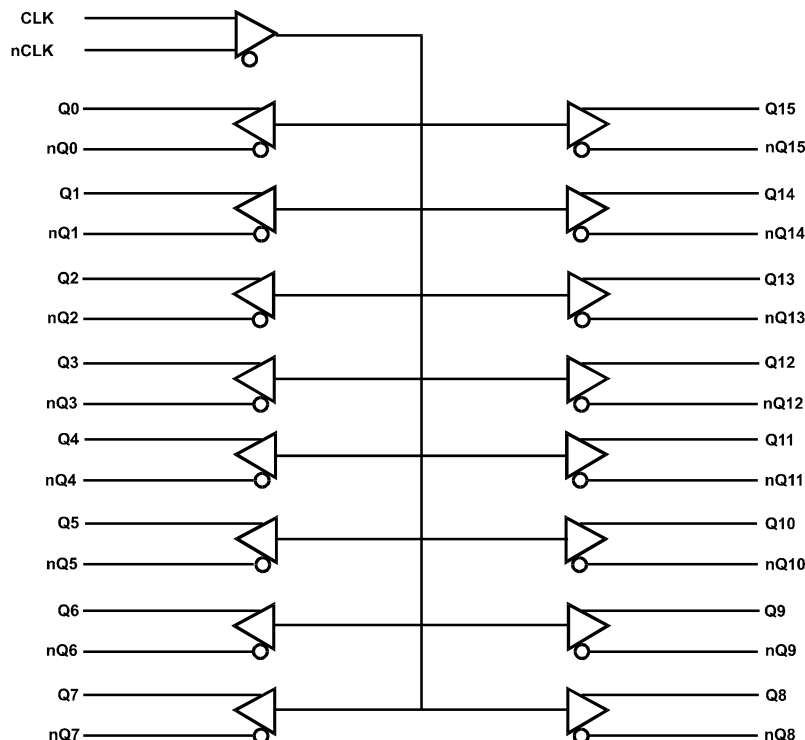


Figure 2. Pin Configuration

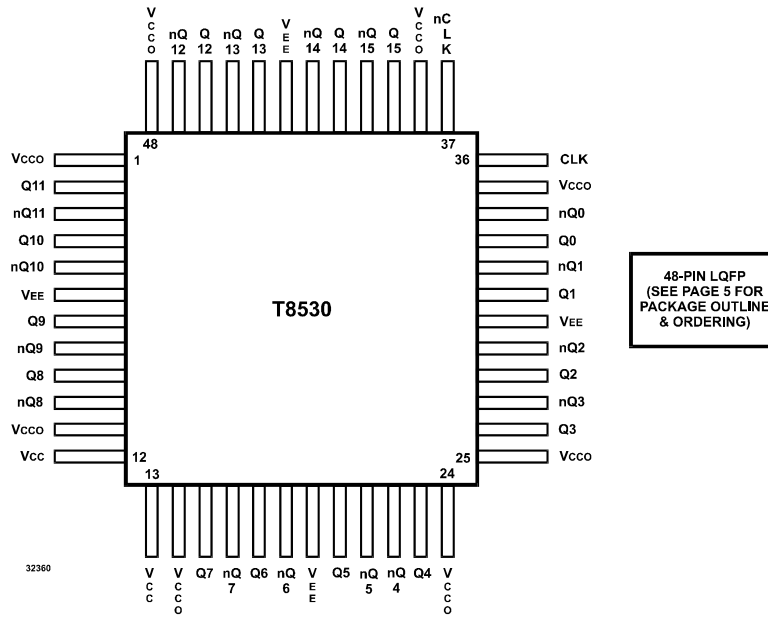


Table 1. Pin Description

Name	Pin #	Type	Description
Vcco	1, 11, 14, 24, 25, 35, 38, 48	P	Output supply, connect to +2.5V
Q11,nQ11	2, 3	O	Differential output pair, 2.5V LVPECL interface level.
Q10, nQ10	4, 5	O	Differential output pair, 2.5V LVPECL interface level.
V <sub>EE</sub>	6, 19, 30, 43	P	Ground, connect to negative supply
Q9,nQ9	7, 8	O	Differential output pair, 2.5V LVPECL interface level.
Q8, nQ8	9, 10	O	Differential output pair, 2.5V LVPECL interface level.
Vcc	12, 13	P	Power supply, connect to +3.3V.
Q7, nQ7	15, 16	O	Differential output pair, 2.5V LVPECL interface level.
Q6, nQ6	17,18	O	Differential output pair, 2.5V LVPECL interface level.
Q5, nQ5	20, 21	O	Differential output pair, 2.5V LVPECL interface level.
Q4, nQ4	22, 23	O	Differential output pair, 2.5V LVPECL interface level.
Q3, nQ3	26,27	O	Differential output pair, 2.5V LVPECL interface level.
Q2, nQ2	28, 29	O	Differential output pair, 2.5V LVPECL interface level.
Q1, nQ1	31, 32	O	Differential output pair, 2.5V LVPECL interface level.
Q0, nQ0	33, 34	O	Differential output pair, 2.5V LVPECL interface level.
CLK	36	I <sub>PD</sub>	Non-inverting differential clock input
NCLK	37	I <sub>PU</sub>	Inverting differential clock input
Q15, nQ15	39, 40	O	Differential output pair, 2.5V LVPECL interface level.
Q14, nQ14	41, 42	O	Differential output pair, 2.5V LVPECL interface level.
Q13, nQ13	44, 45	O	Differential output pair, 2.5V LVPECL interface level.
Q12, nQ12	46, 47	O	Differential output pair, 2.5V LVPECL interface level.

Legend: I = Input  
 O =Output  
 P = Power supply connection  
 I<sub>PD</sub> = Input with pull down (internal)  
 I<sub>PU</sub> = Input with pull up (internal)

Table 2. Pin Characteristics

Symbol	Parameter	Conditions	Min	Typical	Max	Units
C <sub>in</sub>	Input Capacitance				4	pF
R <sub>pullup</sub>	Input Pullup Resistance			50		Kohm
R <sub>pulldown</sub>	Input Pulldown Resistance			50		Kohm

Table 3. Clock Input Function Table

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0:Q15	nQ0:nQ15		
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; V <sub>in</sub> =V <sub>cc</sub> /2	LOW	HIGH	Single Ended to Differential	Non-Inverting
1	Biased; V <sub>in</sub> =V <sub>cc</sub> /2	HIGH	LOW	Single Ended to Differential	Non-Inverting
Biased; V <sub>in</sub> =V <sub>cc</sub> /2	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; V <sub>in</sub> =V <sub>cc</sub> /2	1	LOW	HIGH	Single Ended to Differential	Inverting

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V <sub>cc</sub> /V <sub>cco</sub>	Supply voltage	Referenced to GND			6	V
V <sub>IN</sub>	Input voltage	Referenced to GND	-0.5		V <sub>cc</sub> +0.5V	V
V <sub>OUT</sub>	Output voltage	Referenced to GND	-0.5		V <sub>cco</sub> +0.5V	V
T <sub>STG</sub>	Storage temperature		-65		+150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 5. Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V <sub>cc</sub>	Power Supply Voltage		3.0	3.3	3.6	V
V <sub>cco</sub>	Output Power Supply		2.375	2.5	2.625	V
T <sub>A</sub>	Ambient Temperature		0		+70	°C
I <sub>EE</sub>	Power Supply Current				115	mA

**Table 6. Differential Inputs DC Characteristics**

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +3.0\text{V}$  to  $+3.6\text{V}$ ,  $V_{CCO} = +2.375\text{V}$  to  $+2.625\text{V}$  unless otherwise stated below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{IH}$	Input High Current	nCLK	$V_{in}=V_{CC}=3.6\text{V}$		5	$\mu\text{A}$
		CLK	$V_{in}=V_{CC}=3.6\text{V}$		150	$\mu\text{A}$
$I_{IL}$	Input Low Current	nCLK	$V_{CC}=3.6\text{V}$ , $V_{in}=0\text{V}$	-150		$\mu\text{A}$
		CLK	$V_{CC}=3.6\text{V}$ , $V_{in}=0\text{V}$	-5		$\mu\text{A}$
$V_{PP}$	Peak-to-peak input voltage	CLK, nCLK	0.15		1.3	V
$V_{CMR}$	Common Mode input voltage; Note 1,2	CLK, nCLK	0.05		$V_{CC}-0.85\text{V}$	V

Notes:

1. For single ended applications, the maximum input voltage for CLK and nCLK is  $V_{CC}+0.3\text{V}$
2. Common mode voltage is defined as  $V_{IH}$ .

**Table 7. LVPECL DC Characteristics**

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +3.0\text{V}$  to  $+3.6\text{V}$ ,  $V_{CCO} = +2.375\text{V}$  to  $+2.625\text{V}$  unless otherwise stated below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{OHP}$	Output HIGH Voltage <sup>(1,2)</sup> (Q0:Q15 and nQ0:nQ15 outputs)	$V_{CCO} = +2.5\text{V}$	1100		1500	mV
$V_{OLP}$	Output LOW Voltage <sup>(1,2)</sup> (Q0:Q15 and nQ0:nQ15 outputs)	$V_{CCO} = +2.5\text{V}$	500		800	mV
$V_{swing}$	Peak-to-peak Output Voltage Swing		550		930	mV

Notes:

1. The T8530 is designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket, or mounted on a printed circuit board.
2. Q0:Q15 and nQ0:nQ15 outputs are loaded with 50 ohms to  $V_{CCO}-2$  volts.

**Table 8. AC Characteristics**

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +3.0\text{V}$  to  $+3.6\text{V}$ ,  $V_{CCO} = +2.375\text{V}$  to  $+2.625\text{V}$  unless otherwise stated below.

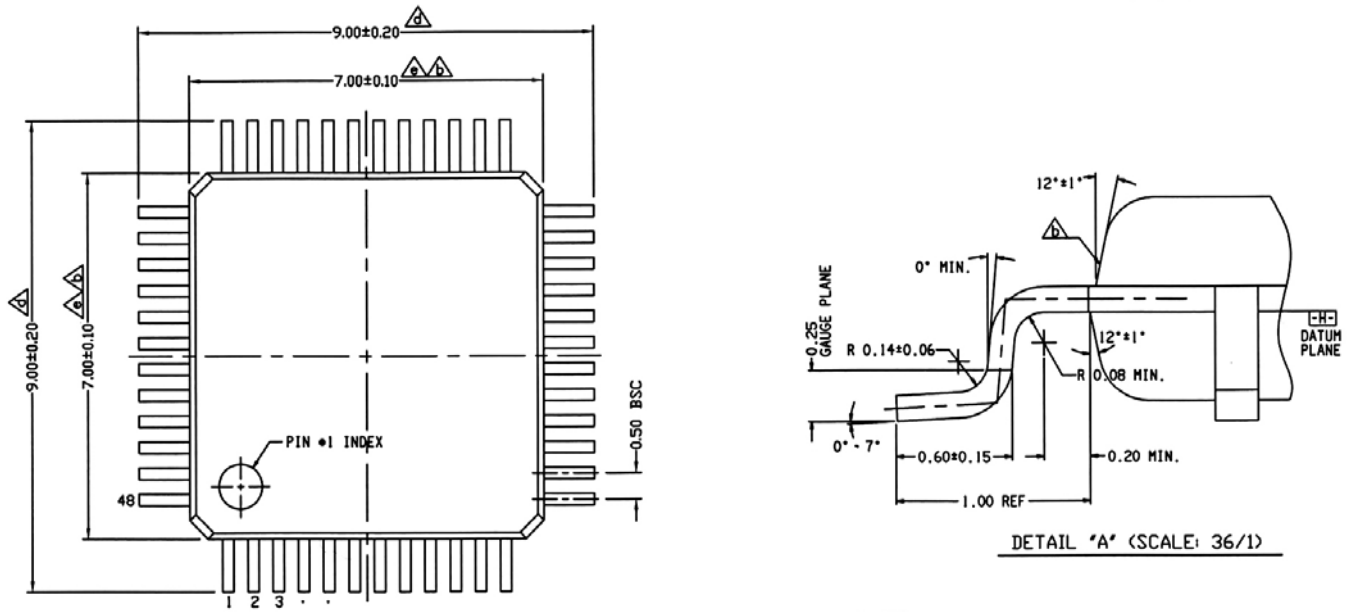
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$f_{max}$	Output Frequency				500	MHz
$t_{Pd}$	Propagation Delay (Note 1)		1		2	ns
$t_{sk(o)}$	Output-to-output Skew (Note 2,4)			26	50	ps
$t_{sk(pp)}$	Part-to-part Skew (Note 3,4)				250	ps
$t_r/t_f$	Output Rise/Fall time (Q, nQ)	20% - 80%	0.3		0.7	ns
$\delta$	Output duty cycle		48		52	%

Notes:

All parameters are measured at 250MHz unless noted otherwise

1. Measured from the  $V_{CC}/2$  of the input to the differential output crossing point
2. Defined as skew between outputs at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
3. Defined as skew between outputs on different parts operating at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
4. This parameter is defined in accordance with JEDEC Standard

Figure 3. Package Outline (48-pin LQFP)



Note: All dimensions are in mm.

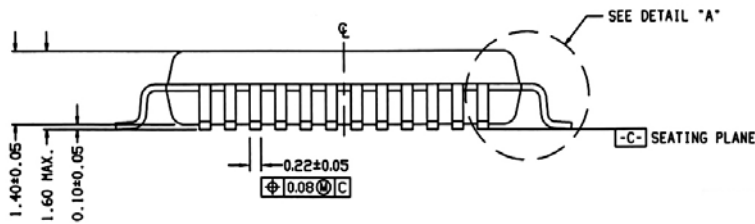


Table 9. Ordering Information

Part Number	Marking	Shipping/Packaging	No. of Pins	Package	Temperature
T8530-DIE	N/A	Waffle Pack	48	N/A	0°C to +70°C
T8530-LQ48	T8530	Trays	48	LQFP	0°C to +70°C