



Low Skew, 1-to-4 LVCMOS/LVTTL to 3.3V LVPECL Fanout Buffer

Applications

- Clock distribution applications in telecommunications, networking and computing systems

General Description

The T853501 is a low skew high performance 1-to-4 LVCMOS/LVTTL to 3.3V LVPECL fanout buffer. The T853501 has two single-ended clock inputs and four LVPECL differential output pairs. The input accepts LVCMOS or LVTTL input levels and translates the inputs to LVPECL level outputs. The clock enable is internally synchronized to eliminate runt clock pulses on the output during asynchronous assertion and de-assertion of the clock enable pin.

Features

- 4 pair of differential 3.3V LVPECL outputs
- Selectable CLK0 and CLK1 inputs for redundant and multiple frequency fanout applications
- Maximum operating frequency: 266MHz
- Output Skew: 30ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 1.9ns (maximum)
- Single +3.3V supply
- 0°C to +70°C ambient operating temperature
- Pin-to-pin compatible with ICS8535-01
- Available as die or in 20-pin TSSOP package

Figure 1. Functional Block Diagram

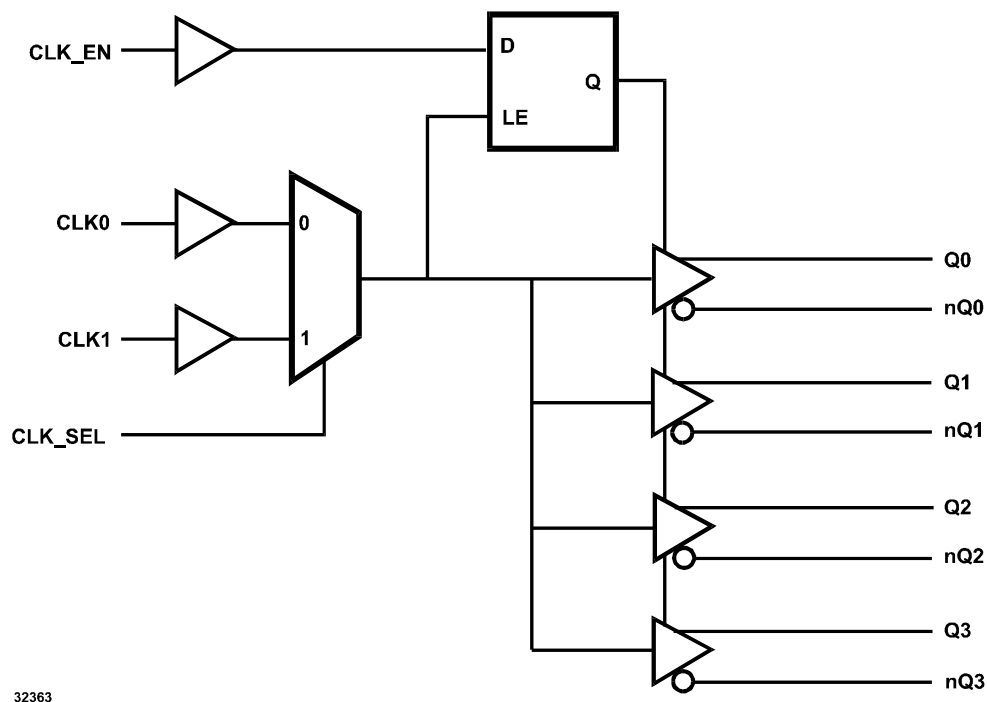
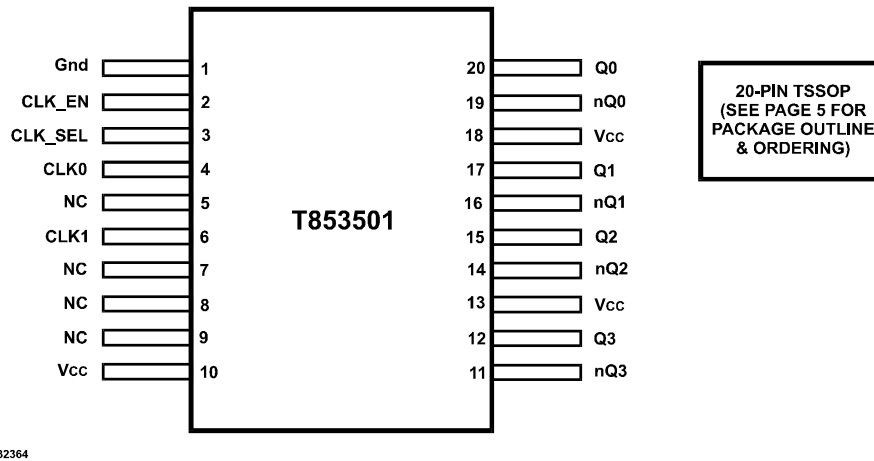


Figure 2. Pin Configuration



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Table 1. Pin Description

Name	Pin #	Type	Description
Gnd	1	P	Connect to ground.
CLK_EN	2	I_PU	Synchronizing clock enable. When high, clock outputs follow clock input. When low, Qx outputs are forced low, nQx outputs are forced high. LVCMOS/LVTTL level with 50K Ohm pull up (internal).
CLK_SEL	3	I_PD	Clock select input. When high, selects CLK1 input. When low, selects CLK0 input. LVCMOS/LVTTL level with 50K Ohm pull down (internal).
CLK0	4	I_PD	LVCMOS/LVTTL clock input with 50K Ohm pull down (internal).
NC	5		No internal connection.
CLK1	6	I_PD	LVCMOS/LVTTL clock input with 50K Ohm pull down (internal).
NC	7		No internal connection.
NC	8		No internal connection.
NC	9		No internal connection.
VCC	10	P	Connect to +3.3V.
nQ3	11	O	Differential output pair, 3.3V LVPECL interface level.
Q3	12	O	
VCC	13	P	Connect to +3.3V.
nQ2	14	O	Differential output pair, 3.3V LVPECL interface level.
Q2	15	O	
nQ1	16	O	Differential output pair, 3.3V LVPECL interface level.
Q1	17	O	
VCC	18	P	Connect to +3.3V.
nQ0	19	O	Differential output pair, 3.3V LVPECL interface level.
Q0	20	O	

Legend: I = Input
 O = Output
 P = Power supply connection
 I_PD = Input with pull down (internal)
 I_PU = Input with pull up (internal)

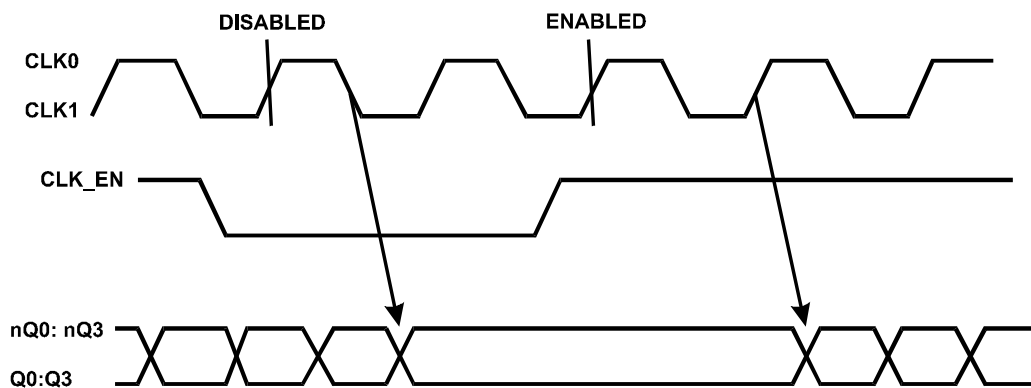
Table 2. Pin Characteristics

Symbol	Parameter	Conditions	Min	Typical	Max	Units
Cin	Input Capacitance				4	pF
R_pullup	Input Pullup Resistance			50		KOhm
R_pulldown	Input Pulldown Resistance			50		KOhm

Table 3. Clock Input Function Table

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Source	Q0:Q3	nQ0:nQ3
0	0	CLK0	Diabld: Low	Diabld: High
0	1	CLK1	Diabld: Low	Diabld: High
1	0	CLK0	Enabled	Enabled
1	1	CLK1	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 3. In the active mode, the state of the outputs are a function of the CLK0 and CLK1 inputs as described in Table 4.



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Figure 3. CLK_EN Timing Diagram

Table 4. Clock Input Function Table

Inputs	Outputs	
	Q0:Q3	nQ0:nQ3
0	Low	High
1	High	Low

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{CC}	Supply voltage	Referenced to GND			6	V
V _{IN}	Input voltage	Referenced to GND	-0.5		V _{CC} +0.5V	V
V _{OUT}	Output voltage	Referenced to GND	-0.5		V _{CC} +0.5V	V
T _{STG}	Storage temperature		-65		+150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 6. Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{CC}	Power Supply Voltage		3.0	3.3	3.6	V
T _A	Ambient Temperature		0		+70	°C
I _{CC}	Power Supply Current				50	mA

Table 7. LVCMOS/LVTTL DC Characteristics

T_A = 0°C to +70°C, V_{CC} = +3.0V to +3.6V unless otherwise stated below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{IH}	Input High Voltage	CLK0, CLK1	2		V _{CC} +0.3	V
		CLK_EN, CLK_SEL	2		V _{CC} +0.3	
V _{IL}	Input Low Voltage	CLK0, CLK1	-0.3		1.3	V
		CLK_EN, CLK_SEL	-0.3		0.8	
I _{IH}	Input High Current	CLK0, CLK1, CLK_SEL			150	uA
		CLK_EN	V _{in} =V _{CC} =3.6V		5	uA
I _{IL}	Input Low Current	CLK0, CLK1, CLK_SEL		-5		uA
		CLK_EN	V _{in} =V _{CC} =3.6V	-150		uA

Table 8. LVPECL DC Characteristics

T_A = 0°C to +70°C, V_{CC} = +3.0V to +3.6V unless otherwise stated below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{OHP}	Output HIGH Voltage ^(1,2) (Q0:Q3 and nQ0:nQ3 outputs)	V _{CC} = 3.3V	2125	2300	2475	mV
V _{OLP}	Output LOW Voltage ^(1,2) (Q0:Q3 and nQ0:nQ3 outputs)	V _{CC} = 3.3V	1350	1500	1650	mV
V _{swing}	Peak-to-peak Output Voltage Swing		600		1000	mV

Notes:

- The T853501 is designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket, or mounted on a printed circuit board.
- Q0:Q3 and nQ0:nQ3 outputs are loaded with 50 ohms to V_{CC}-2 volts.

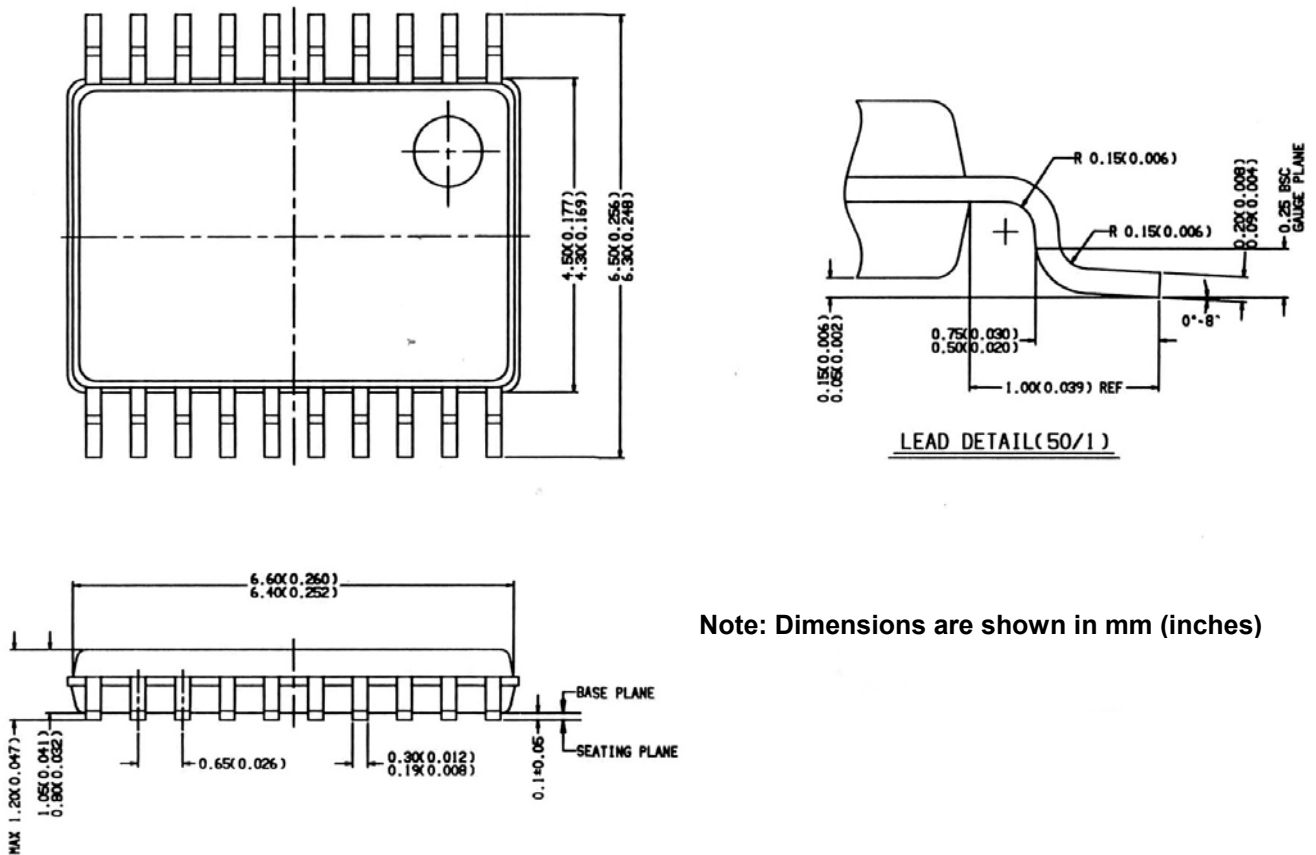
Table 9. AC Characteristics $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC} = +3.0\text{V}$ to $+3.6\text{V}$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{max}	Output Frequency				266	MHz
t_{pd}	Propagation Delay ; Note 1				1.9	ns
$t_{\text{sk}}(\text{o})$	Output-to-output Skew; Note 2,4			11	30	ps
$t_{\text{sk}}(\text{pp})$	Part-to-part Skew, Note 3,4				250	ps
t_r/t_f	Output Rise/Fall time (Q, nQ)	20% - 80%	0.3		0.7	ns
δ	Output duty cycle		48		52	%

Notes:

All parameters are measured at 266MHz unless noted otherwise

1. Measured from the $V_{CC}/2$ of the input to the differential output crossing point
2. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the outputs differential crossing point.
3. Defined as skew between outputs on different parts operating at the same supply voltage and with equal load conditions. Measured at the outputs differential crossing point.
4. This parameter is defined in accordance with JEDEC Standard

Figure 4. Package Outline (20-pin TSSOP)**Table 9. Ordering Information**

Part Number	Marking	Shipping/Packaging	No. of Pins	Package	Temperature
T853501-DIE	N/A	Waffle Pack	20	N/A	0°C to $+70^{\circ}\text{C}$
T853501-TS20	T853501	Tubes	20	TSSOP	0°C to $+70^{\circ}\text{C}$