



## Low Skew, 1-to-4 Differential to 3.3V LVPECL Fanout Buffer

### Applications

- Clock distribution applications in telecommunications, networking and computing systems

### General Description

The T853521 is a low skew, high-performance 1-to-4 Differential to 3.3V LVPECL fanout buffer. The T853521 has two selectable differential clock inputs and four 3.3V LVPECL differential output pairs. The inputs accept most standard differential input levels, and the T853521 translates the input to 3.3V LVPECL level outputs. The clock enable is internally synchronized to eliminate runt clock pulses on the output during asynchronous assertion and de-assertion of the clock enable pin.

### Features

- 4 pair of differential 3.3V LVPECL outputs
- Selectable differential CLK and PCLK inputs
- CLK, nCLK pair accepts LVDS, LVPECL, LVHSTL, SSTL and HCSL input levels
- PCLK, nPCLK pair supports LVPECL, CML and SSTL input levels
- Maximum operating frequency: 650MHz
- Output Skew: 30ps (maximum)
- Part-to-part skew: 150ps (maximum)
- Propagation delay: 1.4ns (maximum)
- Single +3.3V supply
- Pin-to-pin compatible with ICS8533-01
- 0°C to +70°C ambient operating temperature
- Available as die or in 20 pin TSSOP package

Figure 1. Functional Block Diagram

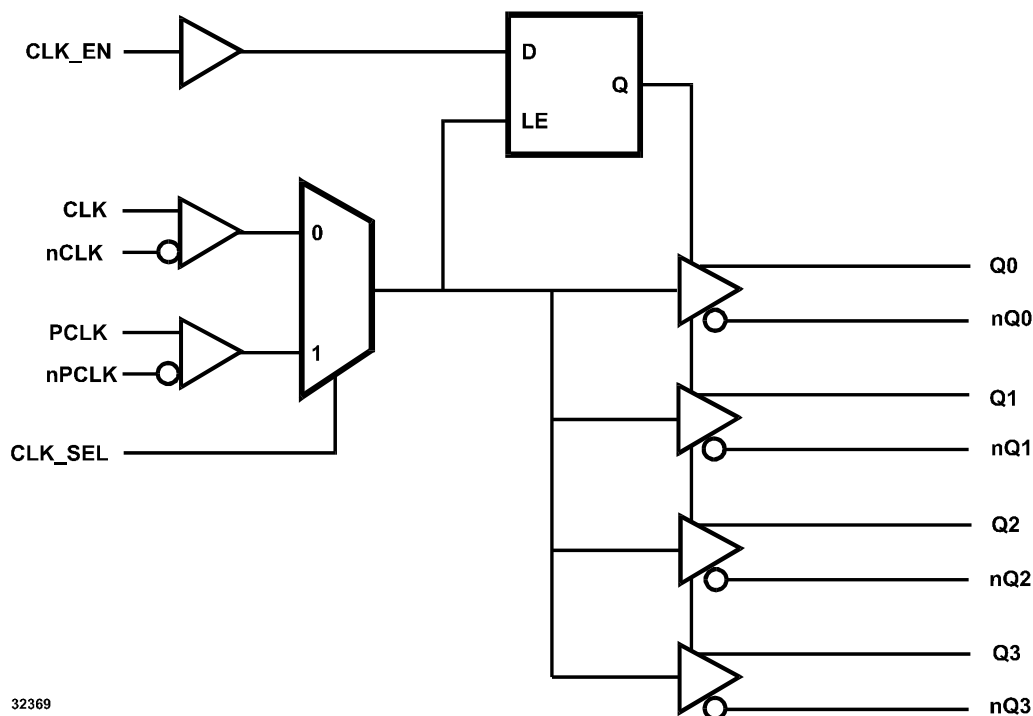
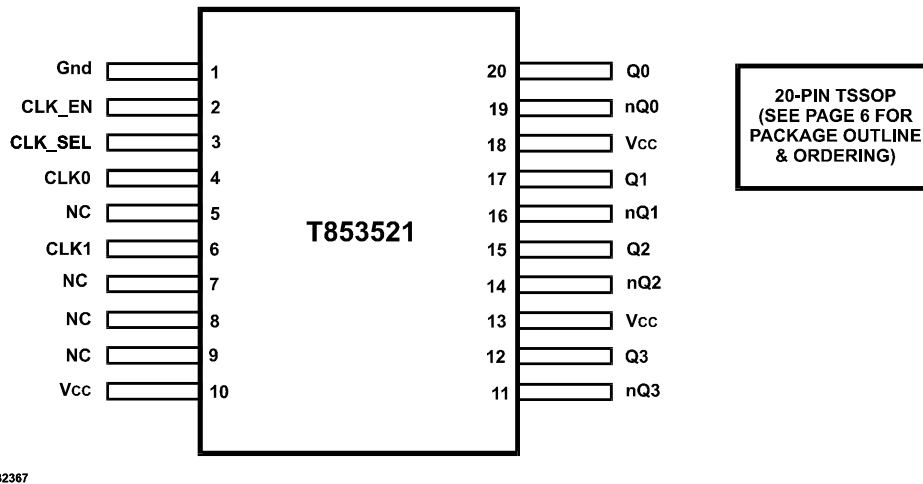


Figure 2. Pin Configuration



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Table 1. Pin Description

Name	Pin #	Type	Description
Gnd	1	P	Connect to ground.
CLK_EN	2	I_PU	Synchronizing clock enable. When high, clock outputs follow clock input. When low, Qx outputs are forced low, nQx outputs are forced high. LVCMOS/LVTTL level with 50K Ohm pull up (internal).
CLK_SEL	3	I_PD	Clock select input. When high, selects CLK1 input. When low, selects CLK0 input. LVCMOS/LVTTL level with 50K Ohm pull down (internal).
CLK	4	I_PD	Non-inverting differential clock input
nCLK	5	I_PU	Inverting differential clock input
PCLK	6	I_PD	Non-inverting differential clock input
nPCLK	7	I_PU	Inverting differential clock input
NC	8		No internal connection.
NC	9		No internal connection.
VCC	10	P	Connect to +3.3V.
nQ3	11	O	Differential output pair, 3.3V LVPECL interface level.
Q3	12	O	
VCC	13	P	Connect to +3.3V.
nQ2	14	O	Differential output pair, 3.3V LVPECL interface level.
Q2	15	O	
nQ1	16	O	Differential output pair, 3.3V LVPECL interface level.
Q1	17	O	
VCC	18	P	Connect to +3.3V.
nQ0	19	O	Differential output pair, 3.3V LVPECL interface level.
Q0	20	O	

Legend: I = Input  
 O = Output  
 P = Power supply connection  
 I\_PD = Input with pull down (internal)  
 I\_PU = Input with pull up (internal)

Table 2. Pin Characteristics

Symbol	Parameter	Conditions	Min	Typical	Max	Units
C <sub>in</sub>	Input Capacitance				4	pF
R <sub>pullup</sub>	Input Pullup Resistance			50		KOhm
R <sub>pulldown</sub>	Input Pulldown Resistance			50		KOhm

Table 3. Control Input Function Table

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Source	Q0:Q3	nQ0:nQ3
0	0	CLK, nCLK	Disabled: Low	Disabled: High
0	1	PCLK, nPCLK	Disabled: Low	Disabled: High
1	0	CLK, nCLK	Enabled	Enabled
1	1	PCLK, nPCLK	Enabled	Enabled

After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 3. In the active mode, the state of the outputs is a function of the CLK, PCLK inputs as described in Table 4.

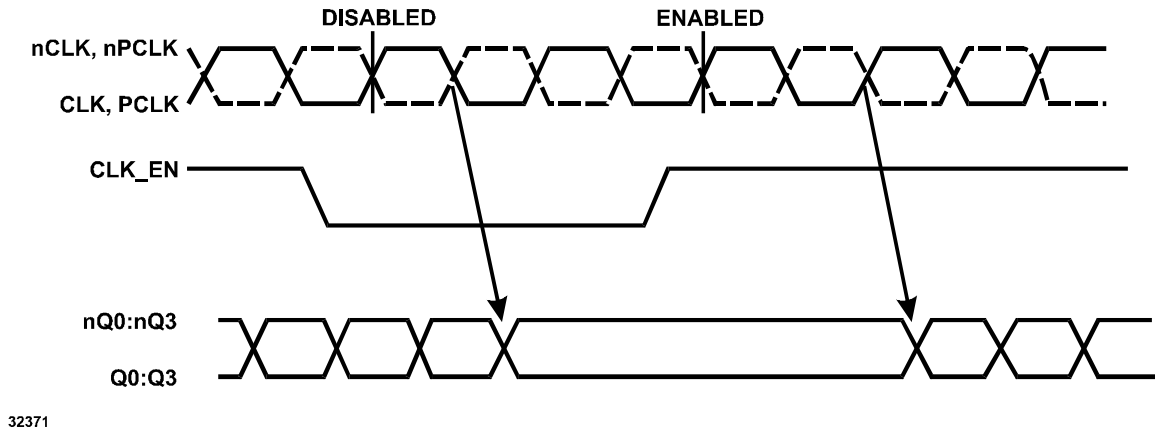


Figure 3. CLK\_EN Timing Diagram

Table 4. Clock Input Function Table

Inputs		Outputs		Input to Output Mode	Polarity
CLK or PCLK	nCLK or nPCLK	Q0:Q3	nQ0:nQ3		
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; Vin=Vcc/2	LOW	HIGH	Single-Ended to Differential	Non-Inverting
1	Biased; Vin=Vcc/2	HIGH	LOW	Single-Ended to Differential	Non-Inverting
Biased; Vin=Vcc/2	0	HIGH	LOW	Single-Ended to Differential	Inverting
Biased; Vin=Vcc/2	1	LOW	HIGH	Single-Ended to Differential	Inverting

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V <sub>CC</sub>	Supply voltage	Referenced to GND			6	V
V <sub>IN</sub>	Input voltage	Referenced to GND	-0.5		V <sub>CC</sub> +0.5V	V
V <sub>OUT</sub>	Output voltage	Referenced to GND	-0.5		V <sub>CC</sub> +0.5V	V
T <sub>STG</sub>	Storage temperature		-65		+150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 6. Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V <sub>CC</sub>	Power Supply Voltage		+3.0	+3.3	+3.6	V
T <sub>A</sub>	Ambient Temperature		0		+70	°C
I <sub>CC</sub>	Power Supply Current				50	mA

Table 7. LVCMOS/LVTTL DC Characteristics

T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = +3.0V to +3.6V unless otherwise stated below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V <sub>IH</sub>	Input High Voltage		2		V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input Low Voltage		-0.3		0.8	V
I <sub>IH</sub>	Input High Current	CLK_SEL	V <sub>in</sub> =V <sub>CC</sub> =+3.6V		150	uA
		CLK_EN	V <sub>in</sub> =V <sub>CC</sub> =+3.6V		5	uA
I <sub>IL</sub>	Input Low Current	CLK_SEL	V <sub>in</sub> =V <sub>CC</sub> =+3.6V	-5		uA
		CLK_EN	V <sub>in</sub> =V <sub>CC</sub> =+3.6V	-150		uA

**Table 8. Differential Inputs DC Characteristics**

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +3.0\text{V}$  to  $+3.6\text{V}$  unless otherwise stated below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
$I_{IH}$	Input High Current	nCLK	$V_{in}=V_{CC}=+3.6\text{V}$			5	$\mu\text{A}$
		CLK	$V_{in}=V_{CC}=+3.6\text{V}$			150	$\mu\text{A}$
		PCLK	$V_{in}=V_{CC}=+3.6\text{V}$			150	$\mu\text{A}$
		nPCLK	$V_{in}=V_{CC}=+3.6\text{V}$			5	$\mu\text{A}$
$I_{IL}$	Input Low Current	nCLK	$V_{CC}=+3.6\text{V}$ , $V_{in}=0\text{V}$	-150			$\mu\text{A}$
		CLK	$V_{CC}=+3.6\text{V}$	-5			$\mu\text{A}$
		PCLK	$V_{CC}=+3.6\text{V}$	-5			$\mu\text{A}$
		nPCLK	$V_{CC}=+3.6\text{V}$	-150			$\mu\text{A}$
$V_{PP}$	Peak-to-peak Voltage	CLK, nCLK		0.15		1.3	V
		PCLK, nPCLK		0.3		1	V
$V_{CMR}$	Common Mode Input Voltage; Note 1,2	CLK, nCLK		0.5		$V_{CC}-0.85\text{V}$	V
		PCLK, nPCLK		1.5		$V_{CC}$	V

Notes:

1. For single ended applications, the maximum input voltage for CLK and nCLK is  $V_{CC}+0.3\text{V}$
2. Common mode voltage is defined as  $V_{IH}$ .

**Table 9. LVPECL DC Characteristics**

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{DD} = +3.0\text{V}$  to  $+3.6\text{V}$  unless otherwise stated below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{OHP}$	Output HIGH Voltage <sup>(1,2)</sup> (Q0:Q3 and nQ0:nQ3 outputs)	$V_{CC} = +3.3\text{V}$	2125	2300	2475	mV
$V_{OLP}$	Output LOW Voltage <sup>(1,2)</sup> (Q0:Q3 and nQ0:nQ3 outputs)	$V_{CC} = +3.3\text{V}$	1350	1500	1650	mV
$V_{swing}$	Peak-to-peak Output Voltage Swing		600		1000	mV

Notes:

1. The T853521 is designed to meet these specifications after thermal equilibrium has been established. The circuit is in a test socket, or mounted on a printed circuit board.
2. Q0:Q3 and nQ0:nQ3 outputs are loaded with 50 ohms to  $V_{CC}-2$  volts.

**Table 10. AC Characteristics**

$T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{CC} = +3.0\text{V}$  to  $+3.6\text{V}$

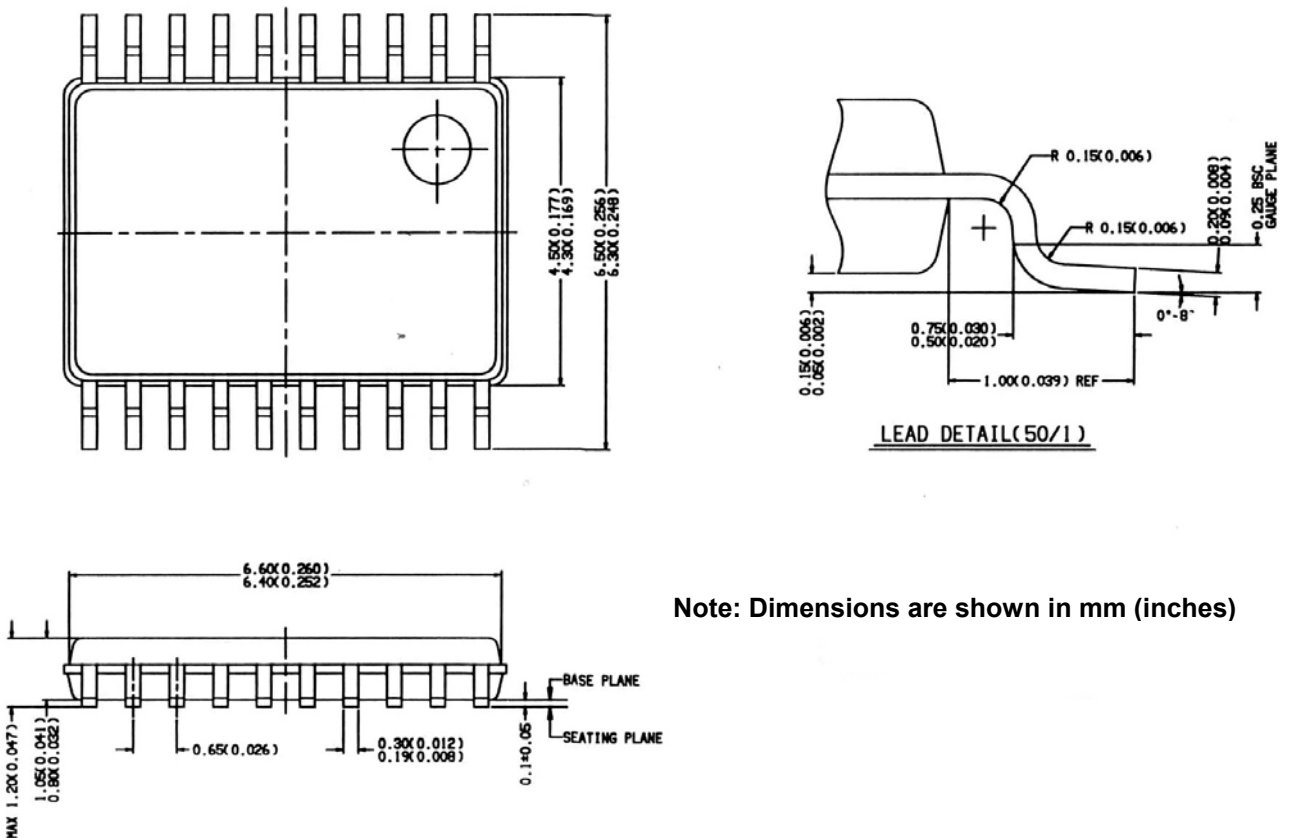
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$f_{\text{max}}$	Output Frequency				650	MHz
$t_{\text{pd}}$	Propagation Delay ; Note 1				1.9	ns
$\text{tsk}(o)$	Output-to-output Skew; Note 2,4				30	ps
$\text{tsk}(pp)$	Part-to-part Skew, Note 3,4				150	ps
$t_r/t_f$	Output Rise/Fall time (Q, nQ)	20% - 80%	0.3		0.7	ns
$\delta$	Output duty cycle		48		52	%

Notes:

All parameters are measured at 500MHz unless noted otherwise

1. Measured from the  $V_{CC}/2$  of the input to the differential output crossing point
2. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the outputs differential crossing point.
3. Defined as skew between outputs on different parts operating at the same supply voltage and with equal load conditions. Measured at the outputs differential crossing point.
4. This parameter is defined in accordance with JEDEC Standard

**Figure 4. Package Outline (20-pin TSSOP)**



Note: Dimensions are shown in mm (inches)

**Table 9. Ordering Information**

Part Number	Marking	Shipping/Packaging	No. of Pins	Package	Temperature
T853521-DIE	N/A	Waffle Pack	20	N/A	$0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$
T853521-TS20	T853521	Tubes	20	TSSOP	$0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$