



Low Skew, 1-to-4 Differential-to-LVDS Fanout Buffer

Applications

- Clock distribution applications in telecommunications, networking and computing systems

General Description

The T854521 is a low skew high performance 1-to-4 Differential to LVDS fanout buffer. The T854521 has two selectable differential clock inputs and four LVDS differential output pairs. The inputs accept most standard differential input level, and T854521 translate the input to LVDS level outputs. The clock enables in internally synchronized to eliminate runt clock pulses on the output during asynchronous assertion and de-assertion of clock enable pin.

Features

- 4 pair of differential LVDS outputs
- Selectable differential CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- PCLK, nPCLK supports the following input types: LVPECL, CML, SSTL
- Maximum output frequency: 800MHz
- Translates any single ended input signal to LVDS levels with resistor bias on nCLK input
- Output skew: 40ps (maximum)
- Part-to-part skew: 500ps (maximum)
- Propagation delay: 2.6ns (maximum)
- 3.3V operating supply
- Pin-to-pin compatible to ICS8543

Figure 1. Functional Block Diagram

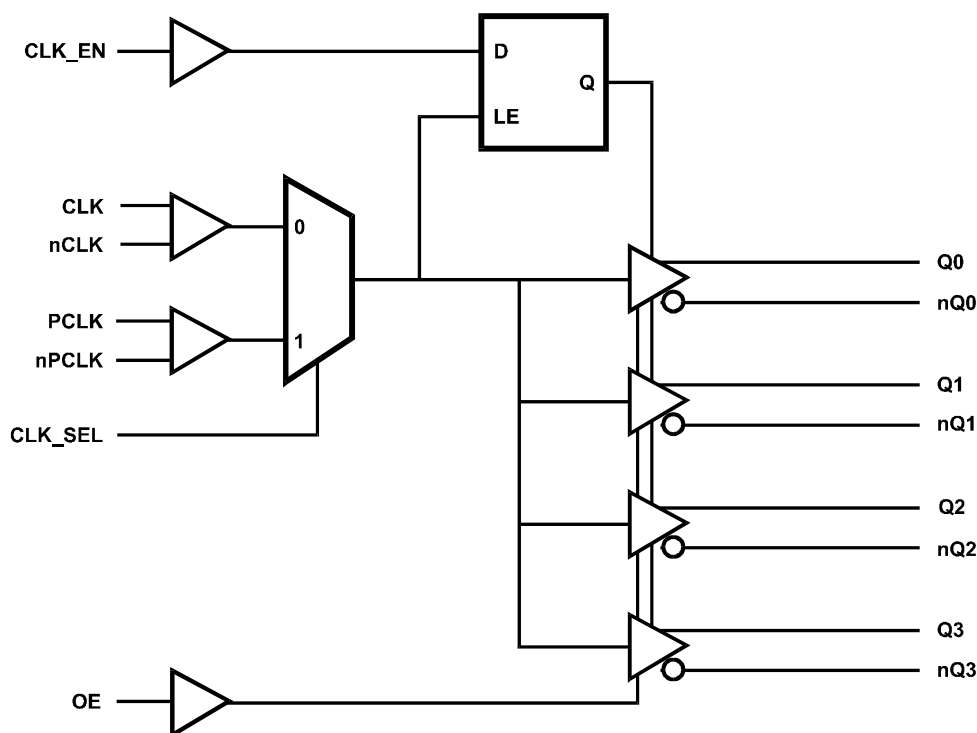
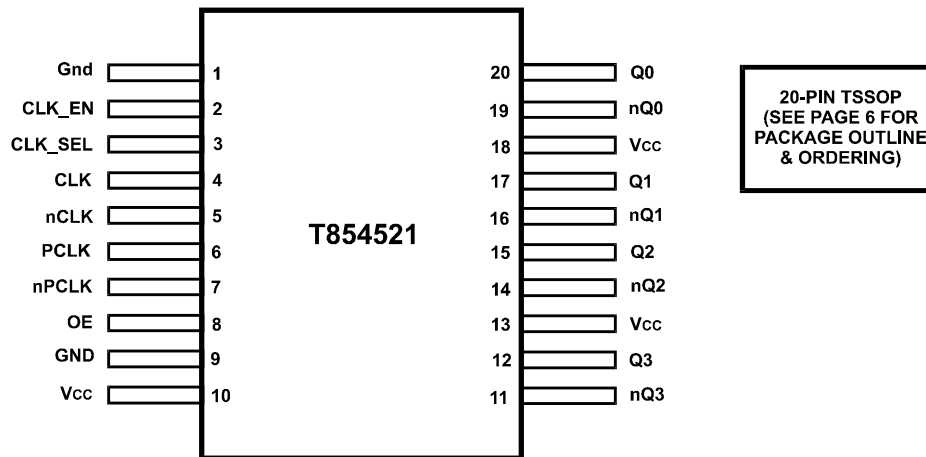


Figure 2. Pin Configuration



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Table 1. Pin Description

Name	Pin #	Type	Description
Gnd	1	P	Connect to ground.
CLK_EN	2	I_PU	Synchronizing clock enable. When high, clock outputs follow clock input. When low, Qx outputs are forced low, nQx outputs are forced high. LVCMOS/LVTTL level with 50KOhm pull up.
CLK_SEL	3	I_PD	Clock select input. When high, selects CLK1 input. When low, selects CLK0 input. LVCMOS/LVTTL level with 50KOhm pull down.
CLK	4	I_PD	Non-inverting differential clock input
nCLK	5	I_PU	Inverting differential clock input
PCLK	6	I_PD	Non-inverting differential clock input
nPCLK	7	I_PU	Inverting differential clock input
OE	8	I_PU	Output enable. Controls enabling and disabling of outputs Q0:Q3 and nQ0:nQ3.
Gnd	9	P	Connect to ground.
VCC	10	P	Connect to +3.3V.
nQ3	11	O	Differential output pair, LVDS interface level.
Q3	12	O	
VCC	13	P	Connect to +3.3V.
nQ2	14	O	Differential output pair, LVDS interface level.
Q2	15	O	
nQ1	16	O	Differential output pair, LVDS interface level.
Q1	17	O	
VCC	18	P	Connect to +3.3V.
nQ0	19	O	Differential output pair, LVDS interface level.
Q0	20	O	

Legend: I = Input
 O = Output
 P = Power supply connection
 I_PD = Input with pull down (internal)
 I_PU = Input with pull up (internal)

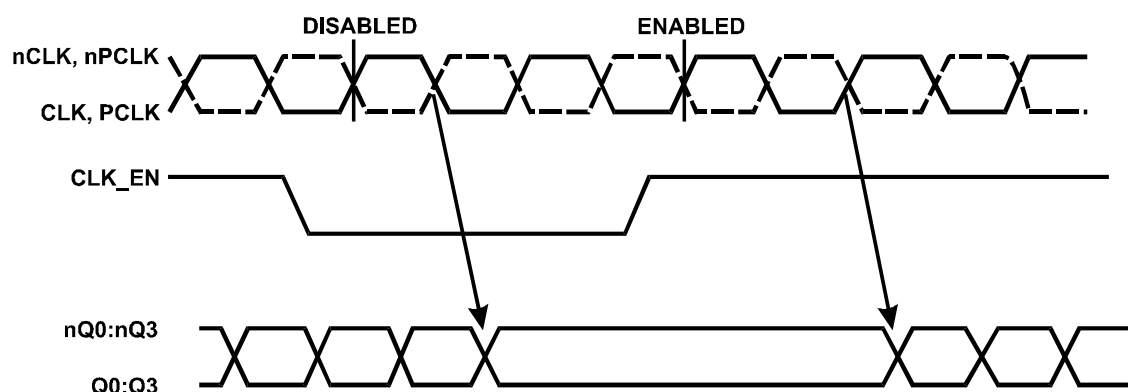
Table 2. Pin Characteristics

Symbol	Parameter	Conditions	Min	Typical	Max	Units
Cin	Input Capacitance				4	pF
R_pullup	Input Pullup Resistance			50		KOhm
R_pulldown	Input Pulldown Resistance			50		KOhm

Table 3. Control Input Function Table

OE	Inputs			Outputs	
	CLK_EN	CLK_SEL	Selected Source	Q0:Q3	nQ0:nQ3
0	X	X		Hi-Z	Hi-Z
1	0	0	CLK, nCLK	Diabled: Low	Diabled: High
1	0	1	PCLK, nPCLK	Diabled: Low	Diabled: High
1	1	0	CLK, nCLK	Enabled	Enabled
1	1	1	PCLK, nPCLK	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 3. In the active mode, the state of the outputs are a function of the CLK, nCLK and PCLK, nPCLK inputs as described in Table 4.



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Figure 3. CLK_EN Timing Diagram

Table 4. Clock Input Function Table

Inputs		Outputs		Input to Output Mode	Polarity
Clk or PCLK	nCLK or nPCLK	Q0:Q3	nQ0:nQ3		
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; Vin=Vcc/2	LOW	HIGH	Single Ended to Differential	Non-Inverting
1	Biased; Vin=Vcc/2	HIGH	LOW	Single Ended to Differential	Non-Inverting
Biased; Vin=Vcc/2	0	HIGH	LOW	Single Ended to Differential	Inverting

Table 5. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{CC}	Supply voltage	Referenced to GND			6	V
V _{IN}	Input voltage	Referenced to GND	-0.5		V _{CC} +0.5V	V
V _{OUT}	Output voltage	Referenced to GND	-0.5		V _{CC} +0.5V	V
T _{STG}	Storage temperature		-65		+150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 6. Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{CC}	Power Supply Voltage		+3.0	+3.3	+3.6	V
T _A	Ambient Temperature		0		+70	°C
I _{CC}	Power Supply Current				50	mA

Table 7. LVCMOS/LVTTL DC Characteristics

T_A = 0°C to +70°C, V_{CC} = +3.0V to +3.6V unless otherwise stated below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V _{IH}	Input High Voltage		2		V _{CC} +0.3	V
V _{IL}	Input Low Voltage		-0.3		1.3	V
I _{IH}	Input High Current	CLK_SEL	V _{in} =V _{CC} =+3.6V		150	uA
		CLK_EN	V _{in} =V _{CC} =+3.6V		5	uA
I _{IL}	Input Low Current	CLK_SEL	V _{in} =V _{CC} =+3.6V	-5		uA
		CLK_EN	V _{in} =V _{CC} =+3.6V	-150		uA

Table 8. LVDS DC Characteristics

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = +3.0\text{V}$ to $+3.6\text{V}$ unless otherwise stated below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OD}	Differential Output Voltage		200	280	360	mV
$D_{V_{OD}}$	Change of V_{OD}				40	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
$D_{V_{OS}}$	Change of V_{OS}			5	25	mV
I_{OZ}	High Impedance Leakage Current		-10		10	mA
I_{OFF}	Power OFF Leakage Current		-20		20	mA
I_{OSD}	Differential Output Short Circuit Current			-3.5	-5	mA
I_{OS}	Output short Circuit Current			-3.5	-5	mA
V_{OH}	Output Voltage High			1.34	1.6	V
V_{OL}	Output Voltage Low		0.9	1.06		V

Table 9. AC Characteristics

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = +3.0\text{V}$ to $+3.6\text{V}$ unless otherwise stated below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{max}	Output Frequency		800			MHz
t_{pd}	Propagation Delay ; Note 1		1.7		2.6	ns
$T_{sk(o)}$	Output-to-output Skew; Note 2,4				40	ps
$T_{sk(pp)}$	Part-to-part Skew, Note 3,4				500	ps
t_r/t_f	Output Rise/Fall time (Q, QN)	20% - 80% @ 50MHz	0.15		0.35	ns
δ	Output duty cycle		45		55	%

Notes:

All parameters are measured at f_{max} unless noted otherwise

1. Measured from the $V_{CC}/2$ of the input to the differential output crossing point
2. Defined as skew between outputs at the same supply voltage and with equal load condition. Measured at $V_{CC}/2$ of the input to the outputs differential crossing point.
3. Defined as skew between outputs on different parts operating at the same supply voltage and with equal load condition. Measured at the outputs differential crossing point.
4. This parameter is defined in accordance with JEDEC Standard

Figure 4. Package Outline (20-pin TSSOP)

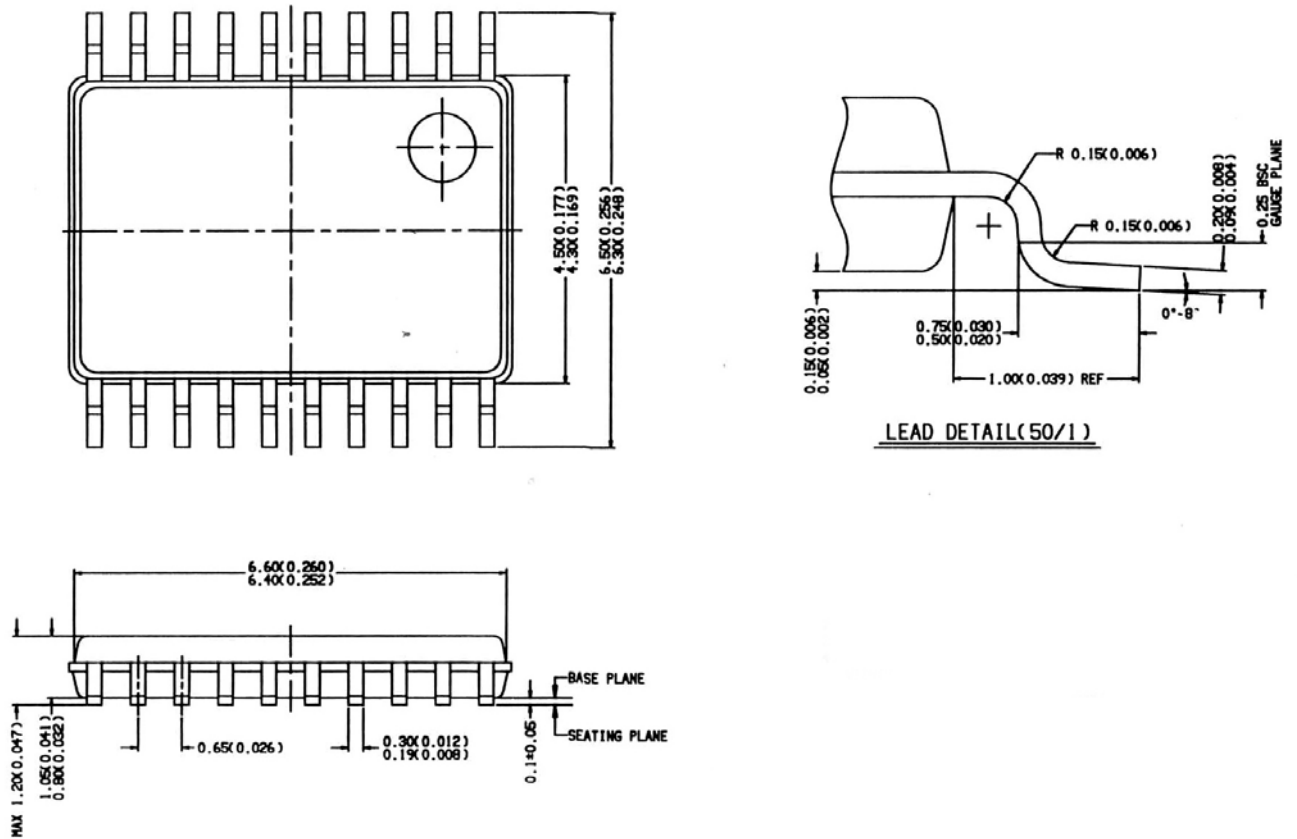


Table 9. Ordering Information

Part Number	Marking	Shipping/Packaging	No. of Pins	Package	Temperature
T854521-DIE	N/A	Waffle Pack	20	N/A	0°C to +70°C
T854521-TS20	T854521	Tubes	20	TSSOP	0°C to +70°C