

Applications

- DVD players and recorders

General Description

The TLSI T98000 is a single-chip, integrated multiple Phase Locked Loop (PLL) clock synthesizer. The device uses an analog Phase Locked Loop (PLL) to accept a 27 MHz crystal input to produce multiple outputs required by DVD Systems. Custom output frequency's are available

Features

- Selectable Audio clocks
- Selectable Processor Clocks
- 27 MHz buffered output clock
- Zero ppm synthesis error in all clocks
- 5V tolerant inputs
- 20-pin, 150 mil SSOP (QSOP)

Figure 1. Functional Block Diagram

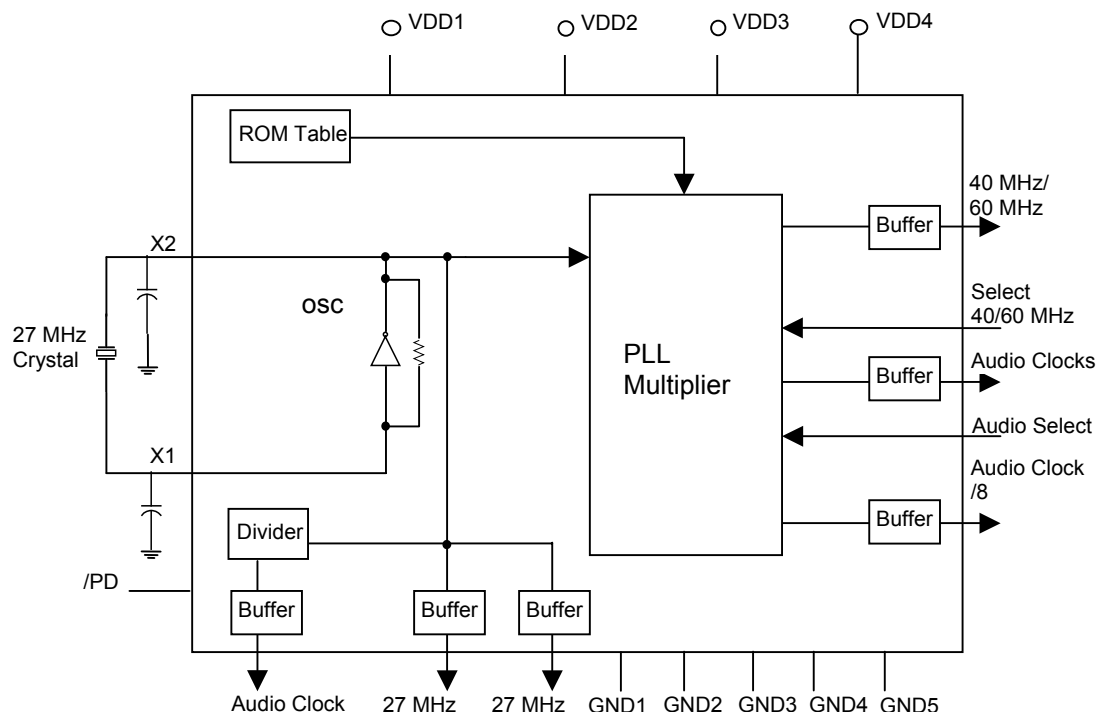


Figure 2. Pin Configuration (Top View)

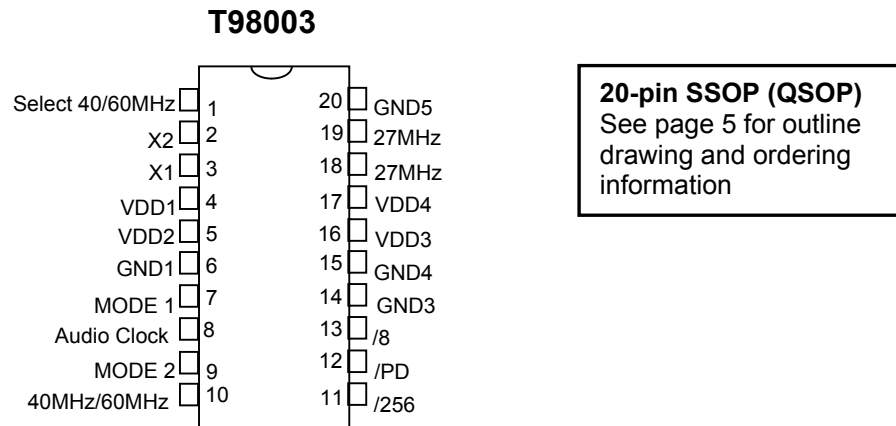


Table 1. Pin Descriptions

Name	Pin #	Type	Description
Select 40/60 MHz	1	I(PU)	Select 40 MHz or 60 MHz output
X2	2	O	Crystal connection. Connect to a 27 MHz crystal
X1	3	I	Crystal connection. Connect to a 27 MHz crystal
VDD1	4	P	Connect to +3.3V
VDD2	5	P	Connect to +3.3V
GND1	6	P	Connect to ground
MODE 1	7	P	Mode control. See Table 2
Audio Clock	8	O	Clock output, Audio Clock
MODE 2	9	I(PU)	Mode control. See Table 2
40 MHz / 60 MHz	10	O	Clock output, 40 MHz or 60 MHz
/256	11	O	Clock output, Audio clock /256
/PD ⁽¹⁾	12	I(PU)	Powerdown control. When LOW, all clocks are disabled
/8	13	O	Clock output, Audio Clock /8
GND3	14	P	Connect to ground
GND4	15	P	Connect to ground
VDD3	16	P	Connect to +3.3V
VDD4	17	P	Connect to +3.3V
27 MHz	18,19	O	27 MHz buffered clock outputs
GND5	20	P	Connect to ground

Legend: I = Input
 O = Output
 P = Power supply connection
 I(PU) = Input with a 250k ohm pull up

Note (1). All disabled clock outputs are tristated (high impedance).

Table 2. Mode Control and Frequency Selection Table (/PD = HIGH) ^(1,2)

Control ⁽³⁾		Outputs		
Pin 7 Mode 1	Pin 9 Mode 2	Pin 8 Audio Clock	Pin 13 /8	Pin 11 /256
0	0	24.576 MHz	3.072 MHz	96.0 kHz
0	1	11.2896 MHz	1.4112 Mhz	44.1 kHz
1	0	8.192 MHz	1.024 Mhz	32.0 kHz
1	1	12.288 MHz	1.536 Mhz	48.0 kHz

Notes: 1. 27MHz (Pins 18 &19) and 24.576 MHz (Pin 8) are active, unless /PD = LOW
 2. 2 kHz standby clock is always active, independent of /PD logic state
 3. 0 = Low, 1 = HIGH

Table 3. Recommended Crystal Specifications

Frequency accuracy is directly proportional to the capacitive load (CL) of the crystal.

Parameter	Definition	Min	Typ	Max	Units
Frequency at CL, FL	Defines the series resonant frequency at CL		27.000		MHz
Total accuracy: includes initial accuracy @ 25°C, aging, and temperature drift (25°C to 70°C)	Maximum deviation from nominal frequency @ 25°C, taking in to account aging, and temperature drift			40	ppm
Load Capacitance CL	Capacitive load for nominal frequency FL		20		pf
C1	Motional capacitance of the crystal			TBD	pf
C0	Shunt capacitance of the crystal			7	pf
ESR	Equivalent Series Resistance of the crystal			40	ohms

Table 4. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Units
Supply voltage, V _{DD}	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Soldering Temperature	Max of 10 seconds			+260	°C
Storage temperature		-65		+150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 5. Operating Conditions

Parameter	Conditions	Min	Typ	Max	Units
Power Supply Voltage, V_{DD}		+3.0	+3.3	+3.6	V
Input High Voltage, V_{IH}		+2.0		V_{DD}	V
Input Low Voltage, V_{IL}				+0.8	V
Operating Temperature, T_A		0	+25	+70	°C

Table 6. DC Electrical Characteristics

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = +3.135\text{ V}$ to $+3.465\text{ V}$

Parameter	Symbol	Min	Typ	Max	Units
Output voltage high $I_{OH} = -8\text{ mA}$	VOH	+2.7			V
Output voltage low $I_{OL} = 8\text{ mA}$	VOL			+0.4	V
Maximum input capacitance (X1,X2)	Cin			3	pF
Power consumption (operating)	I_{dd1}		50		mA
Power consumption (powerdown)	I_{dd2}		TBD		mA

Note:

1. Typical values are at $V_{DD} = 3.3\text{V}$ and 25°C

Table 7. AC Characteristics

All @Cload = 20 pF, $V_{DD} = +3.0\text{V}$ to $+3.6\text{V}$

Parameter	Symbol	Min	Typ	Max	Units
Duty Cycle @ $V_{DD}/2$	δ			45/55	%
Rise time (measured between 0.8V and 2.0V)	Tr	1		2.5	ns
Fall time (measured between 0.8V and 2.0V)	Tf	1		2.5	ns
PLL lock time	Tlock			2.0	ms
Time to clock outputs after VDD is available	Tst			50	ms

Figure 3. Package Outline Drawing (20-pin SSOP/QSOP)

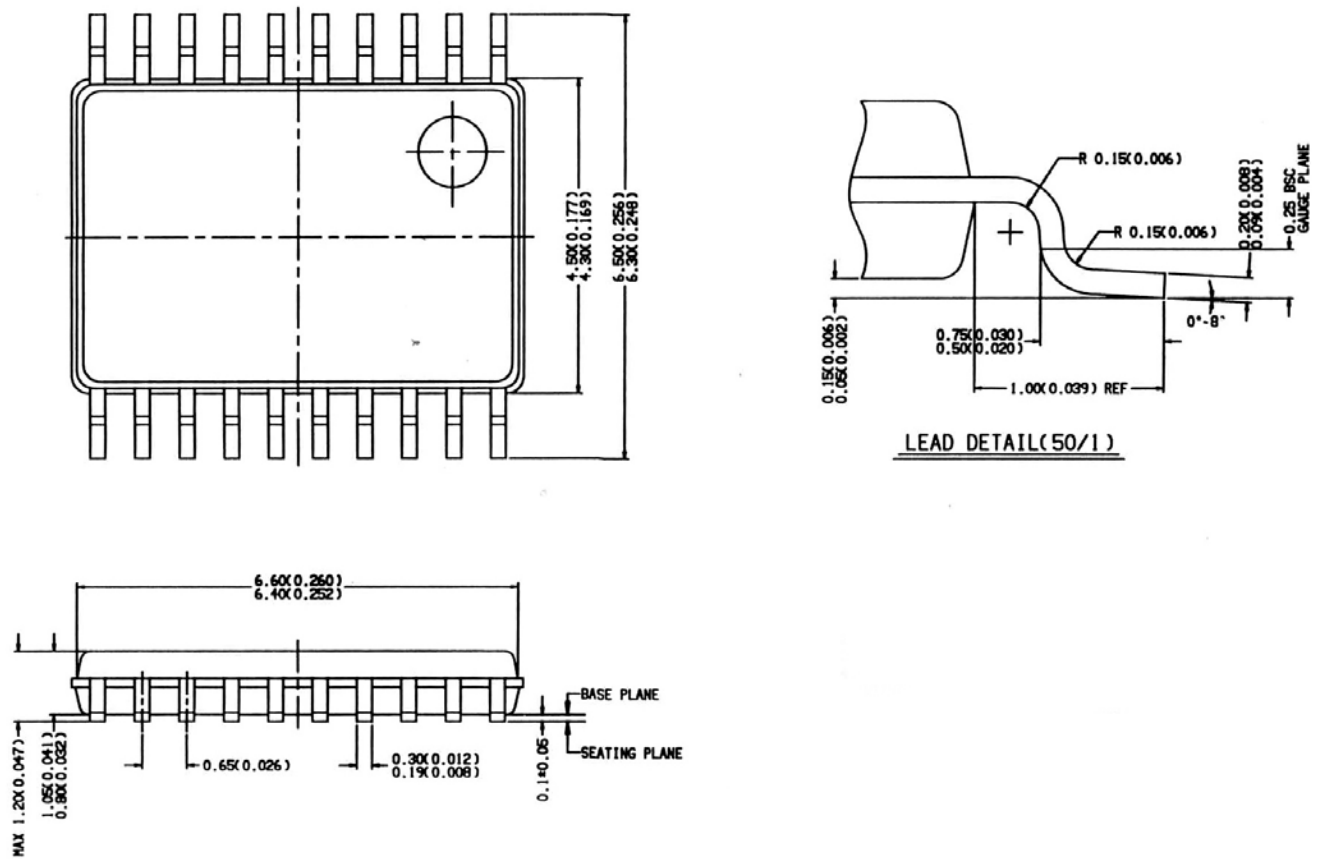


Table 8. Ordering Information

Part Number	Marking	Shipping/Packaging	No. of Pins	Package	Temperature
T98003-SS20	T98003	Tubes	20	SSOP	0°C to +70°C
T98003-SS20-TNR	T98003	Tape & Reel	20	SSOP	0°C to +70°C
T98003-DIE	N/A	Die in Waffle Pack	20	N/A	0°C to +70°C