



T98011

Multi-frequency Clock Synthesizer

Applications

HDTV, Digital TV, Set-top Box Clock Generator

General Description

The TLSI T98011 is a single-chip, integrated multiple Phase Locked Loop (PLL) clock synthesizer. The device uses a analog Phase Locked Loops (PLLs) to convert a single, low cost, 27 MHz fundamental crystal input to multiple outputs at different frequencies with no synthesis errors.

Features

- Switchable 27MHz/74.17582441758 MHz/ 74.25 MHz video decoder clocks
- Standby 27 MHz reference clock
- Two 33 MHz CPU clocks
- Additional 33 MHz clock for video decoder
- Low phase noise for all clocks
- Zero ppm synthesis error for all clocks
- 0°C to +70°C ambient operating temperature range
- 3.3V operation
- 20-pin, 150 mil SSOP (QSOP)

Figure 1. Functional Block Diagram

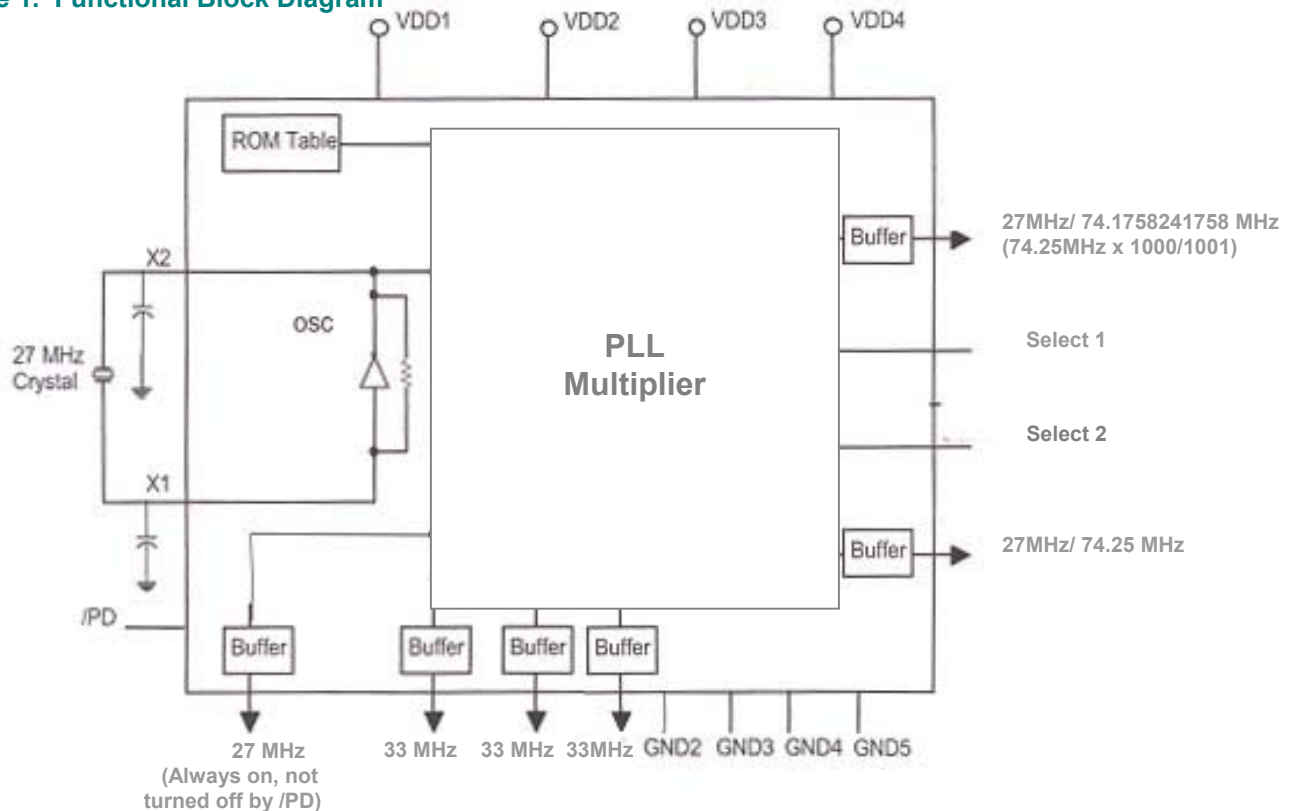
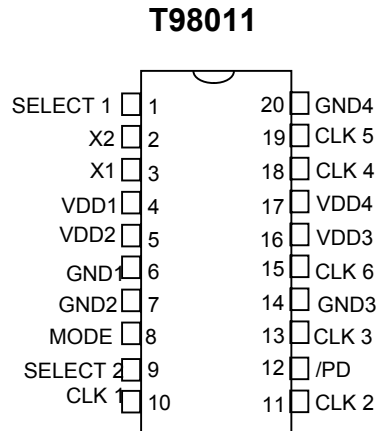


Figure 2. Pin Configuration

**20-pin SSOP (QSOP)**

See page 5 for
package outline and
ordering information

Table 1. Pin Description

Name	Pin #	Type	Description
SELECT 1	1	I	Selects 27 MHz or 74.1758241758 MHz output on pin 10
X2	2	O	Crystal connection. Connect to a 27 MHz crystal
X1	3	I	Crystal connection. Connect to a 27 MHz crystal
VDD1	4	P	Connect to +3.3V
VDD2	5	P	Connect to +3.3V
GND1	6	P	Connect to ground
GND2	7	P	Connect to ground
MODE	8	I	Mode control . See Table 2.
SELECT 2	9	I	Selects 27 MHz or 74.25 MHz output on pin 13
CLK 1	10	O	Clock output, 27 MHz or 74.1758241758 MHz
CLK 2	11	O	Buffered 27 MHz clock output (not gated by /PD pin function)
/PD ⁽¹⁾	12	I(PU)	Powerdown control. When LOW, all clocks are disabled (except CLK 2)
CLK 3	13	O	Clock output, 27 MHz or 74.25 MHz
GND3	14	P	Connect to ground
CLK 6	15	O	33 MHz buffered clock output
VDD3	16	P	Connect to +3.3V
VDD4	17	P	Connect to +3.3V
CLK 4,5	18,19	O	33 MHz buffered clock outputs
GND4	20	P	Connect to ground

Legend: I = Input
 O = Output
 P = Power supply connection
 I(PU) = Input with a 250k ohm pull up

Note (1). All disabled clock outputs are tristated (high impedance).

Table 2. Mode Control and Frequency Selection Table (/PD = HIGH) ^(1,2)

Control ⁽³⁾			Outputs	
Pin 8 Mode	Pin 1 Select 1 (27MHz/74.175MHz)	Pin 9 Select 2 (27MHz/74.25MHz)	Pin 10 CLK 1	Pin 13 CLK 3
0	0	0	27 MHz	27 MHz
0	0	1		74.25 MHz
0	1	0	74.1758241758 MHz	27 MHz
0	1	1		74.25 MHz
1	0	0	Hi Impedance	27 MHz
1	0	1		74.25 MHz
1	1	0	74.1758241758 MHz	Hi Impedance
1	1	1	27 MHz	

- Notes:**
1. 33 MHz (Pins 15, 18 & 19) are active, unless /PD = LOW
 2. 27 MHz standby clock is always active, independent of /PD logic state
 3. 0 = Low, 1 = HIGH

Table 3. Recommended Crystal Specifications

Frequency accuracy is directly proportional to the capacitive load (C_L) of the crystal.

Parameter	Definition	Min	Typ	Max	Units
f_L	Defines the series resonant frequency at C_L		27.000		MHz
Total accuracy: includes initial accuracy @ +25°C, aging, and temperature drift (25°C to 70°C)	Maximum deviation from nominal frequency @ +25°C, taking into account aging, and temperature drift			±40	ppm
Load Capacitance C_L	Capacitive load for nominal frequency, f_L		20		pf
C0/C1	Crystal Gamma	240			-
ESR	Equivalent Series Resistance of the crystal			40	ohms

Table 4. Recommended Operating Conditions

Parameter	Conditions	Min	Typ	Max	Units
Power Supply Voltage, V_{DD}	All V_{DD} pins	3.0	3.3	3.6	V
Input High Voltage, V_{IH}	CMOS levels	2.0		V_{DD}	V
Input Low Voltage, V_{IL}	CMOS levels			0.8	V
Operating Temperature, T_A	Ambient	0	+25	+70	°C

Table 5. Electrical Characteristics

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, All @ $C_L = 20$ pF, $V_{DD} = +3.0\text{V}$ to $+3.6\text{V}$ unless otherwise stated below.

Parameter	Symbol	Min	Typ	Max	Units
Output voltage high $I_{OH} = -8$ mA	VOH	2.8			V
Output voltage low $I_{OL} = 8$ mA	VOL			0.4	V
Maximum input capacitance (X1,X2)	Cin			3	pF
Power consumption (operating), No Load	I_{dd1}		30		mA
Power consumption (powerdown), No Load	I_{dd2}		9		mA

Table 6. Phase Noise Characteristics (crystal phase noise must be less than -130 dBc/Hz @ 10kHz)

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, All @ $C_L = 20$ pF, $V_{DD} = +3.0\text{V}$ to $+3.6\text{V}$ unless otherwise stated below.

Parameter	Symbol	Min	Typ	Max	Units
27 MHz	CLK 1,2,3		-120		dBc/Hz @ 10 kHz
33 MHz	CLK 4,5,6		-100		dBc/Hz @ 10 kHz
74.1758241758 MHz	CLK 1		-100		dBc/Hz @ 10 kHz
74.25 MHz	CLK 3		-100		dBc/Hz @ 10 kHz

Table 7. Output Accuracies (excluding crystal accuracy)

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, All @ $C_L = 20$ pF, $V_{DD} = +3.0\text{V}$ to $+3.6\text{V}$ unless otherwise stated below.

Parameter	Symbol	Min	Typ	Max	Units
27 MHz	CLK 1,2,3			0	ppm
33 MHz	CLK 4,5,6			0	ppm
74.1758241758 MHz	CLK 1			0	ppm
74.25 MHz	CLK 3			0	ppm

Table 8. AC Characteristics

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, All @ $C_L = 20$ pF, $V_{DD} = +3.0\text{V}$ to $+3.6\text{V}$ unless otherwise stated below.

Parameter	Symbol	Min	Typ	Max	Units
Duty Cycle @ $V_{DD}/2$	δ	45	50	55	%
Rise time (measured between 0.8V and 2.0V)	t_r	1		2.5	ns
Fall time (measured between 0.8V and 2.0V)	t_f	1		2.5	ns
PLL lock time	t_{lock}			3	ms
Time to clock outputs after VDD is available	t_{st}			50	ms

Figure 3. Package Outline (20-pin TSSOP/QSOP)

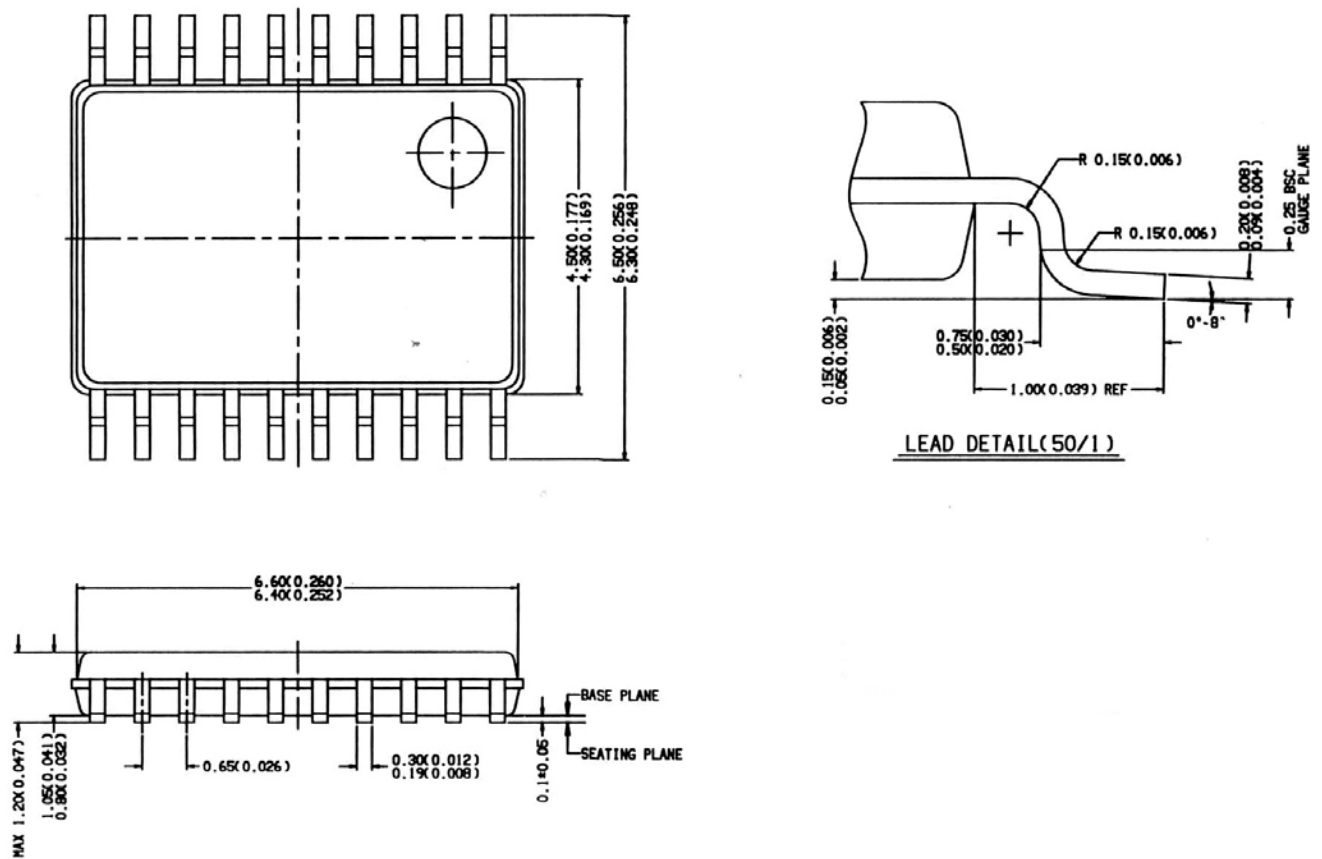


Table 9. Ordering Information

Part Number	Marking	Shipping/Packaging	No. of Pins	Package	Temperature
T98011-Q20	T98011	Tubes	20	QSOP	0°C to +70°C
T98011-Q20-TNR	T98011	Tape & Reel	20	QSOP	0°C to +70°C