



3.3V PLL Clock Multiplier with Reference Clock Output

Applications

- Low cost, general-purpose clock source

General Description

The T98502 is a 3.3V CMOS, clock multiplier integrated circuit. The device provides an excellent quality high frequency output clock from a lower frequency fundamental crystal or clock input. Tri-level selection inputs S0 and S1 are used to select any one of six multipliers, stored in the on-board ROM, and apply it to the input to produce the desired output, up to 220 MHz. In addition, an output, which is a buffered version of the input, is also provided. Phase Locked Loop (PLL) technology allows the device to use an input signal from an inexpensive fundamental crystal.

The T98502, when used with an inexpensive fundamental crystal, provides a cost-effective clock source for most electronic systems.

Features

- Low phase noise
- Zero ppm multiplication error
- Input clock frequency 5 - 50 MHz.
- Input crystal frequency 5 – 27 MHz
- Output clock frequencies up to 220 MHz.
- 3.3V operation with 5V-tolerant inputs and output
- Available lead-free/RoHS-compliant
- Fully compatible with all popular CPUs
- Duty Cycle - 45/55 up to 160 MHz
- 40/60 160 MHz to 220 MHz
- 25mA drive capability at TTL levels
- High-Z output for board level testing
- 0°C to +70°C ambient operating temperature range
- Buffered copy of input clock provided

Figure 1. Functional Block Diagram

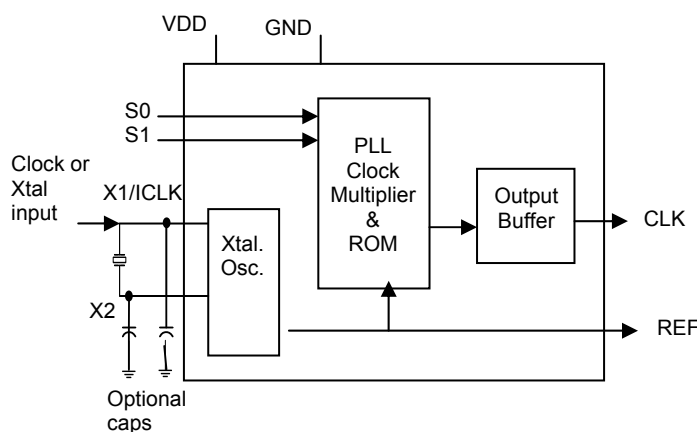


Figure 2. Pin Assignment

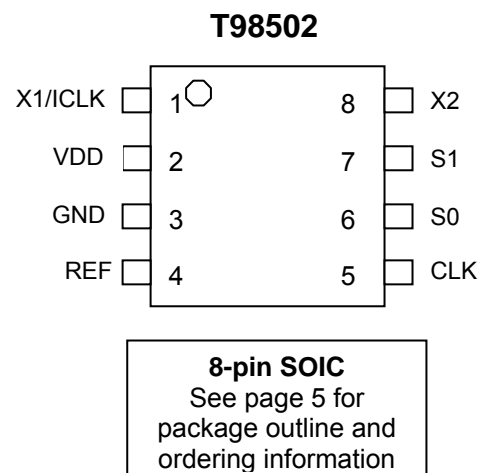


Table 1. Clock Output Table

S1	S0	CLK	Minimum Input
0	0	2 x input	See table 6
0	1	5 x input	See table 6
M	0	3 x input	See table 6
M	1	3.33 x input	See table 6
1	0	4 x input	See table 6
1	1	2.5 x input	See table 6

0 = Connect to ground.

1 = Connect directly to V_{DD}

M = Leave unconnected (floating)

Table 2. Pin Descriptions

No.	Name	Type	Description
1	X1/ICLK	I	Xtal connection or clock input.
2	VDD	P	Connect to +3.3V
3	GND	P	Connect to ground.
4	REF	O	Buffered version of input
5	CLK	O	Clock output per table 1
6	S0	TI	Select pin for output clock. Connect to ground or V_{DD} per Table 1.
7	S1	TI	Select pin for output clock. Connect to ground, V_{DD} or float per Table 1.
8	X2	O	Xtal connection. Leave unconnected for clock input.

Legend:

I = Input

TI = Tri-level Input

O = Output

P = Power supply connection

Table 3. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Units
Supply voltage, V_{DD}	Referenced to GND			4.6	V
Inputs and Clock Outputs	Referenced to GND	-0.5		4.6	V
Soldering Temperature	Max of 10 seconds			+260	°C
Storage temperature		-65		+150	°C

Table 4. Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Operating Temperature	0		+70	°C
Operating Voltage, V_{DD}	+3.0		+3.6	V
Input High Voltage, V_{IH} , X1 CLK only	+2.5			V
Input Low Voltage, V_{IL} , X1 CLK only			+0.5	V
Input High Voltage, V_{IH} , trinary inputs	$V_{DD}-0.5V$			V
Input Low Voltage, V_{IL} , trinary inputs			+0.5	V

Table 5. DC Characteristics

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = +3.0V$ to $+3.6V$ unless otherwise stated below.

Parameter	Condition	Min	Typ	Max	Units
Output High Voltage, V_{OH}	$I_{OH} = -25\text{mA}$	+2.4			V
Output Low Voltage, V_{OL}	$I_{OL} = 25\text{mA}$			+0.4	V
Operating Supply Current, I_{DD} (20 MHz Xtal)	No Load, 100MHz		25		mA
Short Circuit Current	CLK, REF outputs		± 100		mA
Input Capacitance	S0, S1, X1, X2		4		pF
Frequency synthesis error	CLK, REF outputs			0	ppm

Table 6. AC Characteristics

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{DD} = +3.0V$ to $+3.6V$ unless otherwise stated below.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{osc}	Input crystal frequency		5		27	MHz
f_{in}	Input clock frequency		5		50	MHz
f_{out}	Output frequency (CLK) (REF)		24		220	MHz
			5		50	MHz
t_r	Output clock rise time	+0.8 to +2.0V		1		ns
t_f	Output clock fall time	+2.0 to +0.8V		1		ns
t_{od}	Output clock duty cycle (CLK and REF outputs)	1.5 V up to 160 MHz	45	49 to 51	55	%
		160 MHz to 220 MHz	40		60	%
	PLL bandwidth		10			kHz
$t_{jit}(\text{abs})$	Absolute clock period jitter	Deviation from mean $f_{out} = 160\text{ MHz}$		70		ps
$t_{jit}(\text{sigma})$	One sigma clock period jitter	$f_{out} = 160\text{ MHz}$		25		ps

Note 1: External Crystal Connection.

The external crystal should be connected in as close physical proximity to the T98502 as possible. The crystal should be a fundamental mode, parallel resonant crystal. Do not use third overtone. External load capacitors should be fitted in accordance with the crystal manufacturer's specifications.

Note 2: Decoupling and Termination.

Decoupling capacitors of 0.01 μF and 0.1 μF should be connected between V_{DD} and Ground. Capacitors should be mounted as close to the chip as possible. A 33 Ω termination resistor may be connected in series with the clock output in order to minimize ringing and reflections.

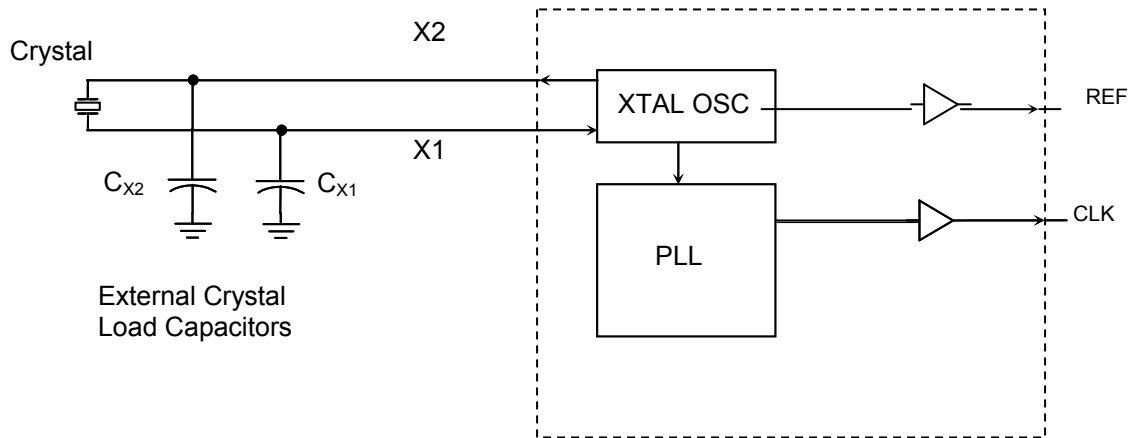
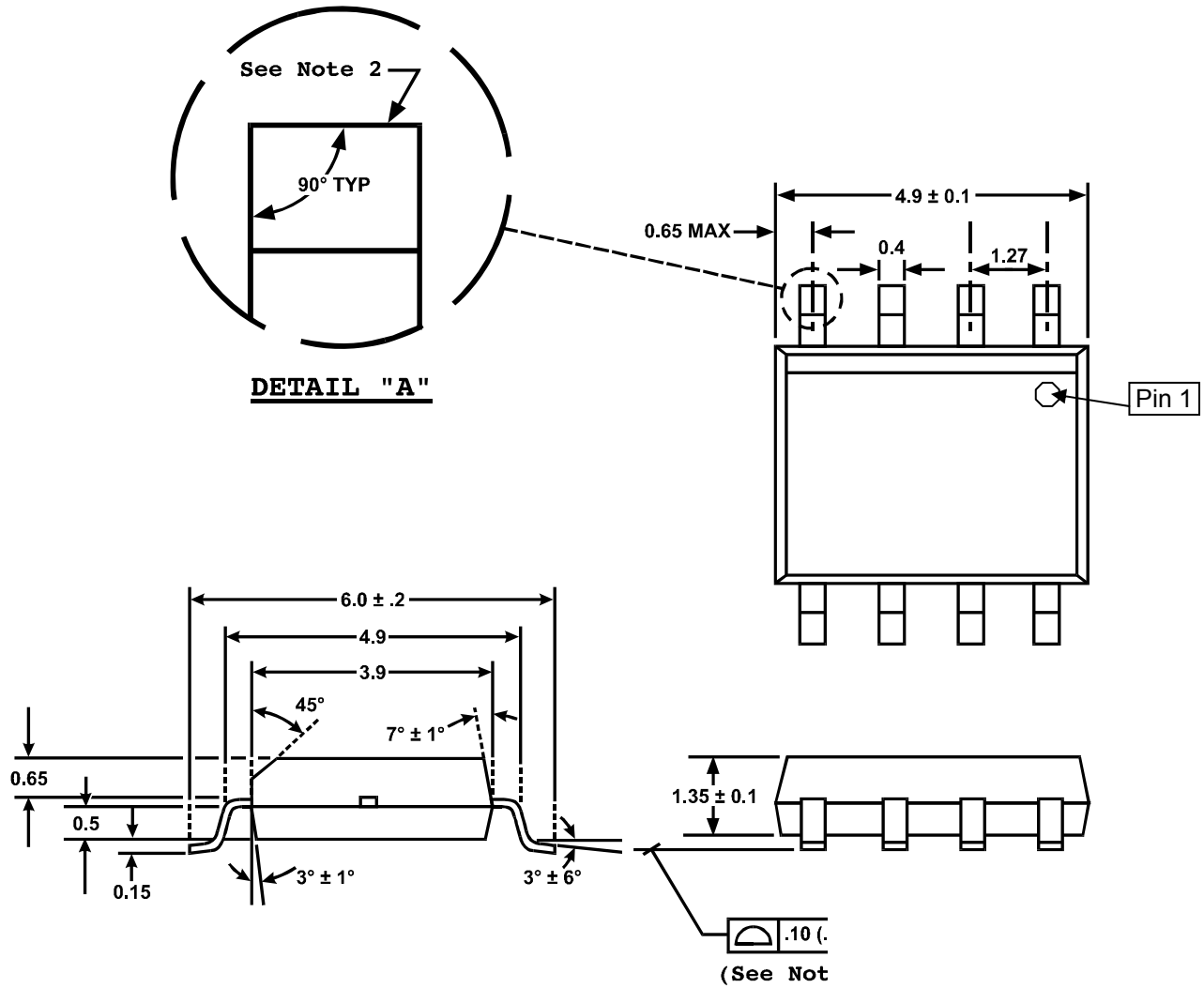
Figure 3. External Crystal Connection Block Diagram

Figure 4. Package Outline (8-pin SOIC)



- Note: 1) All dimensions are in mm.
 2) All leads must be blunt cut. (S
 3) Lead coplanarity not to exceed

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Table 7. Ordering Information

Part Number	Marking	Shipping/Packaging	No. of Pins	Package	Temperature
T98502-SO8	T98502	Tubes	8	SOIC	0°C to +70°C
T98502-SO8-TNR	T98502	Tape & Reel	8	SOIC	0°C to +70°C
T98502-SO8-LF	T98502 •	(Lead Free/RoHS) Tubes	8	SOIC	0°C to +70°C
T98502-SO8-LF-TNR	T98502 •	(Lead Free/RoHS) Tape&Reel	8	SOIC	0°C to +70°C
T98502-DIE		Die in waffle-packs			0°C to +70°C
T98502-DPW		Die in probed wafer			0°C to +70°C