



Low Phase Noise PLL Clock Multiplier 25-200 MHz

Applications

- Clock generation in telecommunications, networking, computing systems and Digital TV
 - SONET/SDH, Fast Ethernet/Gigabit Ethernet, ATM, Fiber Channel, E4 systems, line cards and HTDV

General Description

The T98552 PLL Clock Multiplier is a low phase noise, high-performance clock synthesizer ideally suited for a wide range of applications in which cost, size, power, and jitter need to be optimized. This device is designed to exhibit excellent temperature stability and phase noise performance. The chip accepts a 10 – 27 MHz fundamental mode crystal or clock input and generates output clocks ranging from 25 MHz to 200 MHz. The T98552 includes an internal RC filter that provides low jitter characteristics and internal crystal load capacitors, which eliminate the need for external components.

Features

- +3.3 V operating voltage
- Operating Temperature -40°C to $+85^{\circ}$
- Output frequency range: 25 - 200 MHz
- Input from fundamental crystals: 10–27 MHz
- Input from external clock: 10–27 MHz
- Phase noise: -120 dBc/Hz at 10 kHz offset
- Low jitter: 25 ps (one sigma)
- Nominal Output Duty Cycle 45% to 55%
- Output drives CMOS and TTL loads
- 5V-tolerant inputs and outputs
- Output Enable function tri-states output
- Select inputs (A[2:0]) for multiply ratio of 2, 3, 4, 5, 6, and 8
- Low power, sub-micron CMOS process
- 16-pin SOIC package

- **25 MHz** crystal produces pin selectable **50 MHz, 75MHz, 125 MHz** or **150 MHz** output
- **19.44 MHz** crystal produces pin selectable **38.88 MHz, 58.32 MHz, 77.76 MHz** or **155.52 MHz** output

Figure 1. Functional Block Diagram

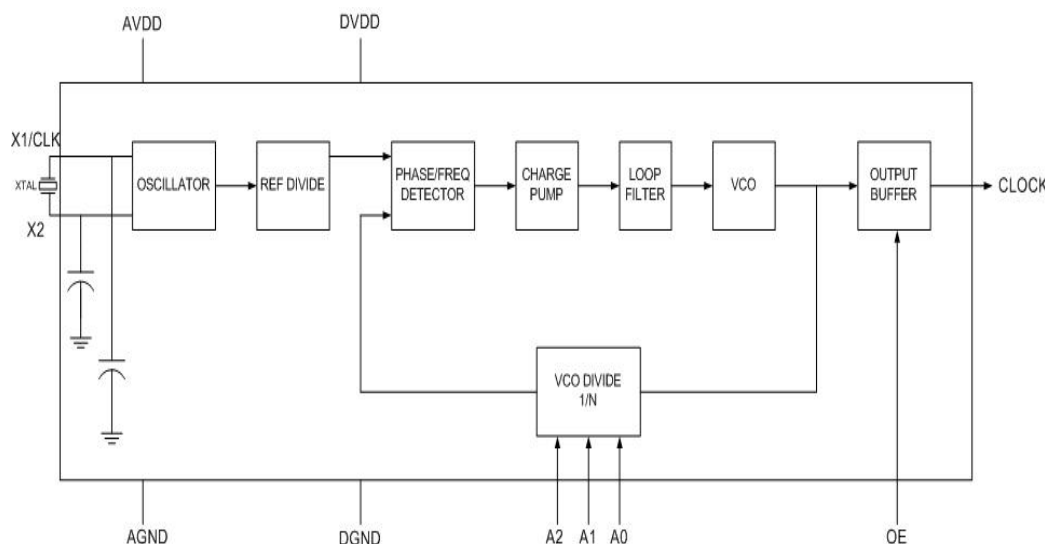
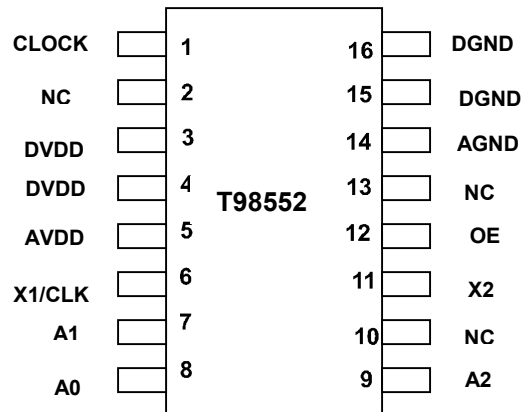


Figure 2. Pin Configuration



16-pin SOIC
See page 5 for outline
drawing and ordering
information.

Table 1. Pin Description

Name	Pin #	Type	Description
CLOCK	1	O	Clock output. Output frequency, $F_o = (\text{multiplier}) \times (\text{input frequency})$.
NC	2	-	No connection
DVDD	3	P	Digital power supply. Connect to +3.3V. Must match all other VDD's.
DVDD	4	P	Digital power supply. Connect to +3.3V. Must match all other VDD's.
AVDD	5	P	Analog power supply. Connect to +3.3V. Must match all other VDD's.
X1/CLK	6	I	Xtal connection. Connect to 10-27 MHz fundamental crystal or CLK input
A1	7	I_PU	Multiplier select pin 1. Determines CLOCK output. See table 2.
A0	8	I_PU	Multiplier select pin 0. Determines CLOCK output. See table 2.
A2	9	I_PU	Multiplier select pin 2. Determines CLOCK output. See table 2.
NC	10	-	No connection
X2	11	I	Xtal connection. Connect to 10-27 MHz fundamental crystal.
OE	12	I_PU	Output enable. Tri-sates CLOCK output when low.
NC	13	-	No connection
AGND	14	P	Analog ground. See page 4 for specific recommendations.
DGND	15	P	Digital ground. See page 4 for specific recommendations.
DGND	16	P	Digital ground. See page 4 for specific recommendations..

Legend: I = Input
O = Output
P = Power supply connection
I_PU = Input with pull up (internal)

Table 2. Clock Output Function Table

OE	Multiplier Select Inputs			CLOCK Output
	A2	A1	A0	
0	DC ⁽¹⁾	DC ⁽¹⁾	DC ⁽¹⁾	Output Disabled
1	0	0	0	2 x input frequency
1	0	0	1	3 x input frequency
1	0	1	0	4 x input frequency
1	0	1	1	6x input frequency
1	1	0	0	5x input frequency
1	1	0	1	8 x input frequency
1	1	1	0	See note (2)
1	1	1	1	See note (2)

Notes:

- (1) DC = Don't care.
(2) For these select input combinations, CLOCK output defaults to 2 x input frequency.

Table 3. Commonly Used Frequencies

Fast Ethernet & Gigabit Ethernet Frequencies							
CLOCK output (MHz)	25	50	62.5	75	100	125	155.52
Crystal Required (MHz)	12.5	10	12.5	25	25	25	19.44
Multiplier	2	5	5	3	4	5	8
SONET/SDH Frequencies				Fiber Channel		E4	ATM
CLOCK output (MHz)	38.88	77.76	155.52	53.125	106.25	139.264	149.76
Crystal Required (MHz)	19.44	19.44	19.44	10.625	21.25	17.408	18.72
Multiplier	2	4	8	5	5	8	8

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AVDD/DVDD	Power supply voltage	Referenced to GND			6	V
V _{IN}	Input voltage	Referenced to GND	-0.5		VDD+0.5V	V
V _{OUT}	Output voltage	Referenced to GND	-0.5		VDD+0.5V	V
T _{STG}	Storage temperature		-65		+150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 5. Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AVDD/DVDD	Power Supply Voltage		2.7	3.3	5.5	V
T _A	Ambient Temperature		-40		+85	°C

Table 6. DC Characteristics

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, AVDD/DVDD = +3.135V to +3.465V, unless otherwise stated below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High level output voltage (CMOS level)	$I_{OH} = -4\text{ mA}$	VDD-0.4			V
V_{OH}	High level output voltage (TTL level)	$I_{OH} = -12\text{ mA}$	2.4			V
V_{OL}	Low level output voltage	$I_{OL} = 12\text{ mA}$			0.4	V
V_{IH}	High level input voltage		2.0			V
V_{IL}	Low level input voltage				0.8	V
I_{DD}	Operating supply current	No load, 100 MHz		15	22	mA
I_{SC}	Short circuit current	CLOCK output		± 50		mA
I_{XTAL}	Input DC current, X1			2	4	mA
C_{IN}	Input capacitance	OE, A0,A1,A2		4		pF

Table 7. AC Characteristics

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, AVDD/DVDD = +3.135V to +3.465V, unless otherwise stated below.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{XTAL}	Crystal frequency range		10		27	MHz
f_{CLK}	CLK input frequency range		10		27	MHz
f_{OUT}	Output Frequency		25		200	MHz
δ	Output duty cycle	$25\text{ MHz} < f_{OUT} < 160\text{ MHz}$	45		55	%
		$160\text{ MHz} \leq f_{OUT} < 200\text{ MHz}$	40		60	%
$t_{JI}(\text{abs})$	Maximum absolute jitter	No load, $f_{OUT} = 100\text{ MHz}$		± 50	± 75	ps
$t_{JI}(\text{sigma})$	One sigma clock jitter	No load, $f_{OUT} = 100\text{ MHz}$		± 18	± 25	ps
t_R/t_F	Output CLOCK Rise/Fall time	No load, 20% - 80% VDD			1.5	ns
N_{PH}	Phase Noise, relative to carrier	1 KHz offset		-110		dBc/Hz
		10 KHz offset		-120		dBc/Hz

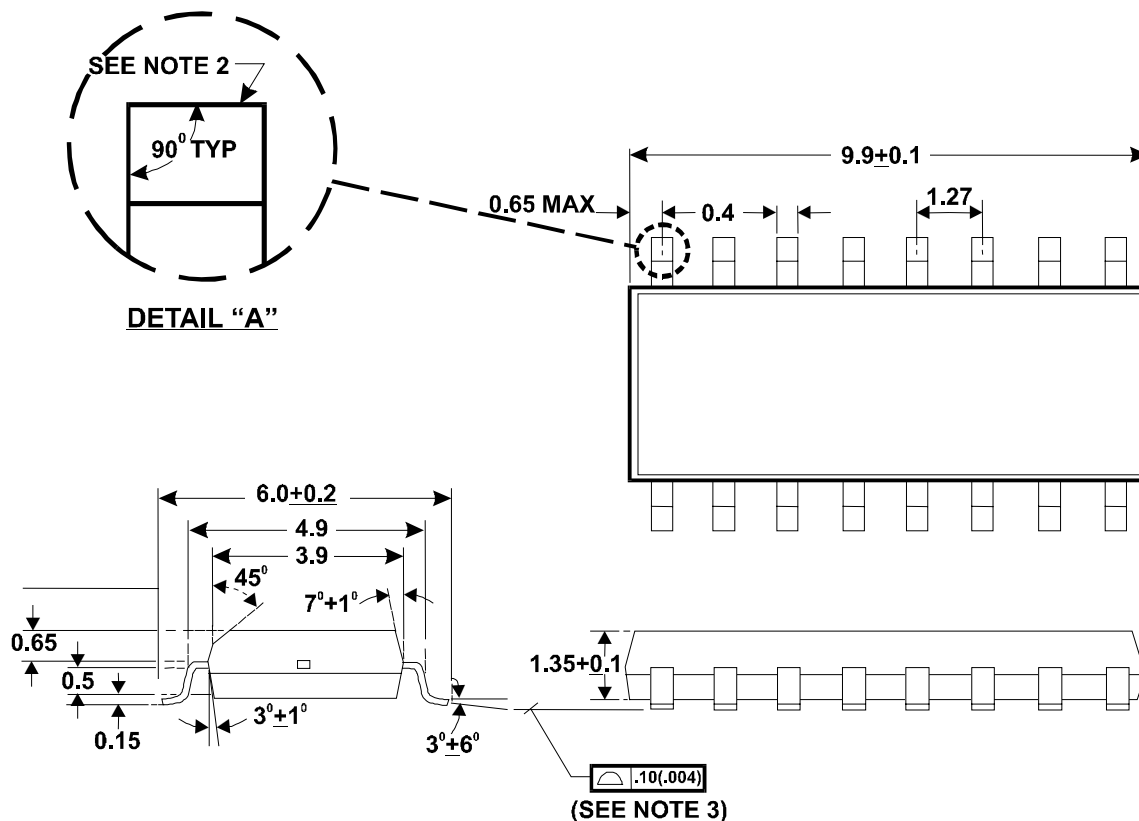
Implementation Recommendations for Low Phase Noise

In order to achieve the specified performance, decoupling capacitors of $0.1\mu\text{F}$ in parallel with $0.01\mu\text{F}$ should be connected between AVDD and AGND as well as between DVDD and DGND. These should be as close as possible to the analog and digital power supply pins on the device.

Crystal Selection

The crystal (Xtal) should be located as close as possible to the input pins X1/CLK (pin 6) and X2 (pin 11). The trace length between the crystal and the T98552 input pins should be kept to a minimum to avoid unwanted parasitic inductance and capacitance. Other signal traces should not be routed near the crystal traces. The crystal should be fundamental mode and parallel resonant.

Figure 3. Package Outline (16-pin SOIC)



NOTE: 1) ALL DIMENSIONS ARE IN MM.

2) ALL LEADS MUST BE BLUNT CUT.
(SEE DETAIL "A")

3) LEAD COPLANARITY NOT TO EXCEED 0.004" MAXIMUM.

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Table 8. Ordering Information

Part Number	Marking	Shipping/Packaging	No. of Pins	Package	Temperature
T98552-SO16	T98552	Tubes	16	SOIC	-40°C to +85°C
T98552-SO16-TNR	T98552	Tape & Reel	16	SOIC	-40°C to +85°C
T98552-DIE	N/A	Die in Waffle Packs	16	N/A	-40°C to +85°C
T98552-DPW	N/A	Die in Probed Wafer	16	N/A	-40°C to +85°C