

100-400 MHz, PLL Timing Generator with LVDS outputs

Applications

- High-speed serial data communications such as:
 - Gigabit Ethernet, Fibre Channel, ICSI, SONET/SDH, Infiniband, Hyper-transport,
 - PCI Express, SPI 4.2, Serial ATA

General Description

The T98553 PLL Timing Generator IC is a low phase noise, high performance, LVDS frequency synthesizer ideally suited for a wide range of applications in which cost, size, power, and jitter need to be minimized. This IC is designed to exhibit excellent temperature stability and phase noise performance. The chip accepts a 10–27 MHz fundamental mode crystal input and generates LVDS output clocks ranging from 100 MHz to 400 MHz. The T98553 includes an internal RC filter that provides low jitter characteristics and crystal load capacitors, which eliminate the need for external components.

Features

- Differential LVDS output
- Output frequency range: 100 - 400 MHz
- Input from fundamental crystals: 10–27 MHz
- Phase noise: –100 dBc/Hz at 1 kHz offset
- Low jitter: 25 ps (one sigma)
- Nominal output duty cycle: 45% to 55%
- 5V-tolerant inputs and outputs
- Output enable function tri-states output
- Select input ADIVB for multiply ratio of 8 and 16
- Low power, sub-micron CMOS process
- +3.3V supply voltage, capable of operating at +2.7V
- Operating temperature -40°C to +85°

Figure 1. Functional Block Diagram

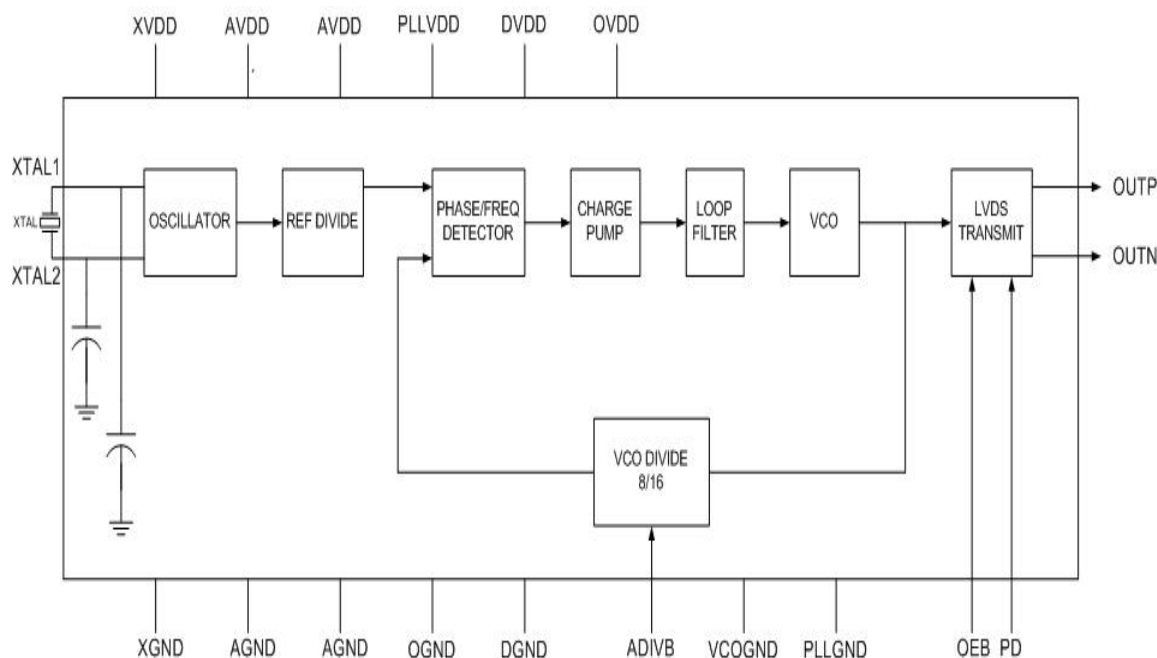
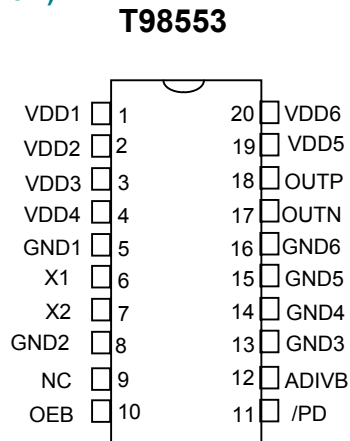


Figure 2. Pin Configuration (Top View)



20-pin SSOP (QSOP)
See page 5 for
package outline and
ordering information

Table 1. Pin Description

Name	Pin #	Type	Description
VDD1	1	P	Connect to +3.3V
VDD2	2	P	Connect to +3.3V
VDD3	3	P	Connect to +3.3V
VDD4	4	P	Connect to +3.3V
GND1	5	P	Connect to ground
X1	6	I	Crystal connection. Connect to a 27 MHz crystal
X2	7	I	Crystal connection. Connect to a 27 MHz crystal
GND2	8	P	Connect to ground
NC	9	NC	Do not connect
OEB	10	I(PD)	Output Enable (active low)
/PD ⁽¹⁾	11	I(PD)	Power down control. When HIGH, all clock outputs are disabled.
ADVIB	12	I(PU)	Multiplier Select. Determines output's multiplier 8/16. Internal pull-up.
GND3	13	P	Connect to ground
GND4	14	P	Connect to ground
GND5	15	P	Connect to ground
GND6	16	P	Connect to ground
OUTN, OUTP	17,18	O	LVDS differential clock outputs
VDD5	19	P	Connect to +3.3V
VDD6	20	P	Connect to +3.3V

Legend: I = Input
O = Output
P = Power supply connection
I(PU) = Input with a 250k ohm pull up
I(PD) = Input with a >50k ohm pull down

Note (1): All disabled clock outputs are tri-stated (high impedance).

Table 2. Power Down and Frequency Multiplier Selection Table

ADIVB (Pin 12)	/PD (Pin 11)	OUTP / OUTN (Pins 18, 17)
0	0	$f_{xtal} \times 8$
0	1	Disabled (High-Impedance)
1	0	$f_{xtal} \times 16$
1	1	Disabled (High-Impedance)

Notes: 0 = LOW, 1 = HIGH

Table 3. Recommended Crystal Specifications

Frequency accuracy is directly proportional to the capacitive load (C_L) of the crystal.

Parameter	Definition	Min	Typ	Max	Units
f_{xtal}	Defines the fundamental resonant frequency at C_L	10		27	MHz
Total accuracy: includes initial accuracy @ +25°C, aging, and temperature drift (25°C to 70°C)	Maximum deviation from nominal frequency @ +25°C, taking into account aging, and temperature drift			±50	ppm
Load Capacitance C_L	Capacitive load for nominal frequency f_{xtal}		20		pf
$C_0/C_1^{(1)}$	Crystal Gamma			240	--
ESR	Equivalent Series Resistance of the crystal			40	ohms

Notes: (1) C_0 is the shunt capacitance of the crystal
 C_1 is the motional capacitance of the crystal

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD1-6}	Power supply voltage	Referenced to GND			6.0	V
V_{IN}	Input voltage	Referenced to GND	-0.3		$V_{DD}+0.3V$	V
V_{OUT}	Output voltage	Referenced to GND	-0.3		$V_{DD}+0.3V$	V
T_{STG}	Storage temperature		-65		+150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 5. Recommended Operating Conditions

Parameter	Conditions	Min	Typ	Max	Units
Power Supply Voltage, VDD	All VDD pins	+2.7	+3.3	+5.0	V
Input High Voltage, V_{IH}	CMOS levels	+2.0		VDD	V
Input Low Voltage, V_{IL}	CMOS levels			+0.8	V
Operating Temperature, T_A	Ambient	-40	+25	+85	°C

Table 6. DC Electrical Characteristics

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = +3.3\text{V} \pm 5\%$ unless otherwise stated below.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Current	I_{IN}	ADIVB/OEB/PD		10	200	μA
Input Current, X1	I_{XTAL}			2	4	mA
Input capacitance	C_{IN}	ADIVB/OEB/PD		4		pF
Power Supply Current (operating)	I_{DD}	No Load, 200 MHz		18	25	mA
Power consumption (power down)	I_{PD}	/PD "HIGH"		8		mA
Power Consumption (output disabled)	I_{OEB}	OEB "HIGH"		11		mA
Short Circuit Current	I_{SC}	OUTN, OUTP		± 50		mA

Table 7. AC Characteristics

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, All @ $C_L = 20\text{ pF}$, $V_{DD} = +3.3\text{V} \pm 5\%$ unless otherwise stated below.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Crystal Frequency Range	f_{xtal}		10		27	MHz
Output Frequency	f_{OUT}		100		400	MHz
Output Duty Cycle	δ	@ $V_{DD}/2$	45	48-52	55	%
Maximum Absolute Jitter	$t_{ji}(\text{abs})$	$f_{OUT} = 200\text{ MHz}$		± 50	± 75	ps
One Sigma Clock Jitter	$t_{ji}(\text{sigma})$	$f_{OUT} = 200\text{ MHz}$			25	ps
Phase Noise @ 1 KHz offset	N_{PH}	Relative to Carrier		-110 ⁽¹⁾		dBc/Hz
Phase Noise @ 10 KHz offset	N_{PH}	Relative to Carrier		-120 ⁽¹⁾		dBc/Hz
Output Enable Time	t_{EN}	OEB high to OUTP, N on			50	ns
Output Disable Time	t_{DIS}				50	ns
PLL lock time	t_{lock}				3	ms
Time to clock outputs after VDD is available	t_{st}				50	ms

Notes: (1) Crystal phase noise must be less than -130 dBc/Hz @ 10kHz

Table 8. DC Electrical Characteristics for LVDS Outputs

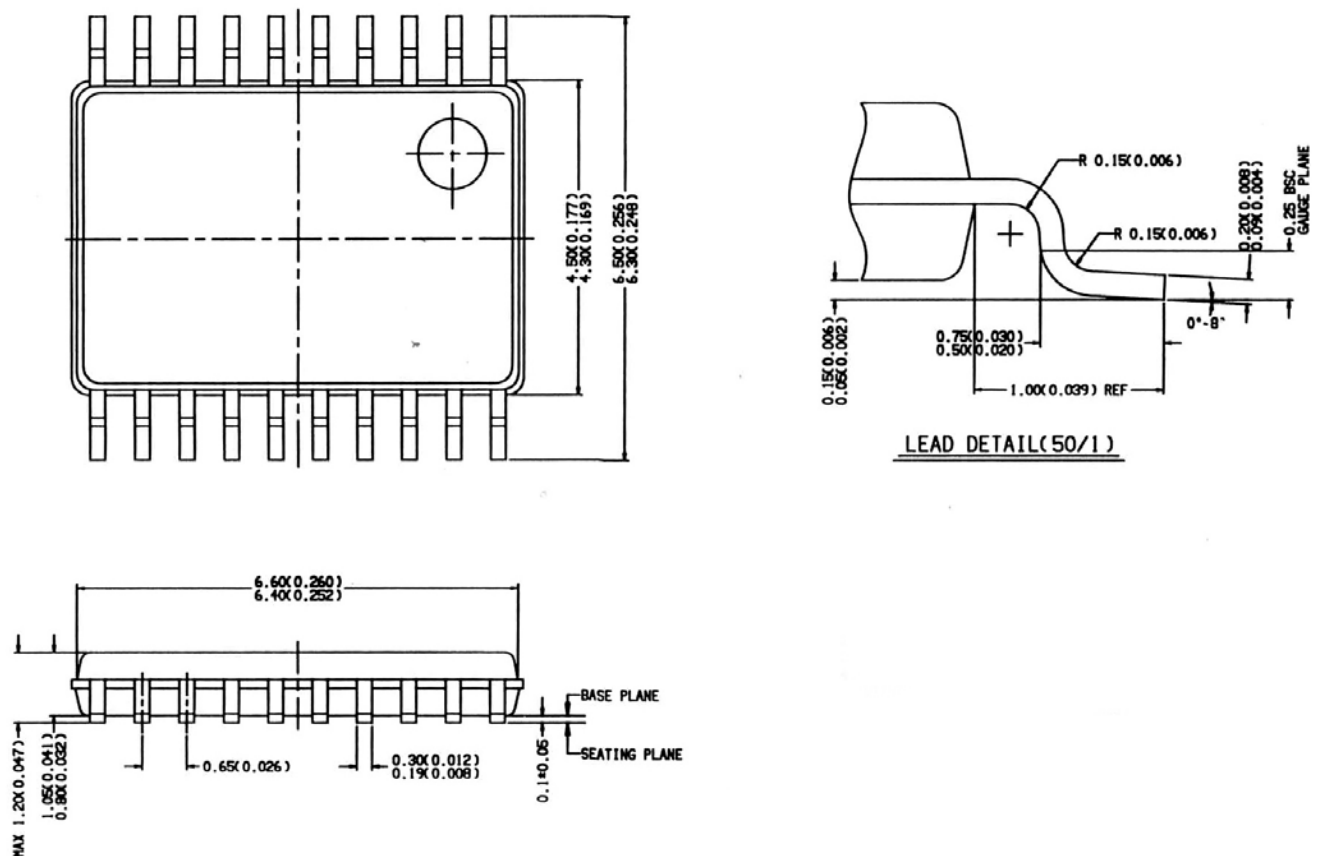
$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = +3.3\text{V} \pm 5\%$ unless otherwise stated below.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Differential Voltage	V_{OD}	$R_L = 100\ \Omega$	250	450	600	mV
V_{OD} Magnitude Change	ΔV_{OD}	$R_L = 100\ \Omega$	-50		+50	mV
Output High Voltage	V_{OH}	$R_L = 100\ \Omega$		1.4	1.6	V
Output Low Voltage	V_{OL}	$R_L = 100\ \Omega$	0.9	1.1		V
Offset Voltage	V_{OS}	$R_L = 100\ \Omega$	1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}	$R_L = 100\ \Omega$	0	3	25	mV
Power-off Leakage	I_{OXD}	$V_{out} = V_{DD}$ or GND		1	10	μA
Output Short Circuit Current	I_{OSC}			-5.7	-8	mA

Table 9. AC Switching Characteristics for LVDS Outputs

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, All @ $C_L = 10$ pF, $V_{DD} = +3.3\text{V} \pm 5\%$ unless otherwise stated below.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Differential Output Rise Time	t_R	$R_L = 100 \Omega$	0.15		1.0	ns
Differential Output Fall Time	t_F	$R_L = 100 \Omega$	0.15		1.0	ns
Differential Output Signal Symmetry	D.C.	$R_L = 100 \Omega$	40		80	%
Maximum Operating Frequency	f_{MAX}			400		MHz
Output Skew	t_{skew}				± 10	ps

Figure 3. Package Outline (20-pin SSOP/QSOP)**Table 9. Ordering Information**

Part Number	Marking	Shipping/Packaging	No. of Pins	Package	Temperature
T98553-SS20	T98553	Tubes	20	SSOP	-40°C to $+85^\circ\text{C}$
T98553-SS20-TNR	T98553	Tape & Reel	20	SSOP	-40°C to $+85^\circ\text{C}$
T98553-DIE	N/A	Die in Waffle Packs	20	N/A	-40°C to $+85^\circ\text{C}$
T98553-DPW	N/A	Die in Probed Wafer	20	N/A	-40°C to $+85^\circ\text{C}$